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CHARGE-COUPLED DEVICES  
FOR ANALOG SIGNAL PROCESSING --  
A CIRCUIT STUDY

Maxwell Douglas Biddle

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## Monterey, California



# THESIS

CHARGE-COUPLED DEVICES  
FOR ANALOG SIGNAL PROCESSING --  
A CIRCUIT STUDY

by

Maxwell Douglas Biddle, Jr.

Thesis Advisor:

Tien Fan Tao

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March 1976

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Charge-Coupled Devices  
for Analog Signal Processing --  
a Circuit Study

by

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Submitted in partial fulfillment of the  
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL  
March 1976



## ABSTRACT

The operation of a two-phase charge-coupled shift register is discussed and analyzed. A parametric study for simultaneous operation with more than one input signal is presented. The output circuit is analyzed for its contribution to non-linearity. An analog signal processing linear model of the charge-coupled device is proposed.



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## I. INTRODUCTION

Charge-coupled semiconductor devices (CCD's) were invented in 1970 at the Bell Laboratories [Ref. 1]. Since their invention and initial experimental investigation, they have held forth promise of low noise, high dynamic range, analog delay lines. Great effort has been successfully expended to develop charge-coupled devices into self-scanned solid-state image sensors. The devices are held to be attractive for analog and digital signal processing and digital memory. The simpler fabrication of charge-coupled as opposed to Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or bipolar transistor technologies promises increased production yields to manufacturers. The net result is a quickening interest in charge-coupled devices for signal processing.

### A. CHARGE-COUPLED SEMICONDUCTOR DEVICES

Charge-coupled semiconductor devices consist of closely spaced MOS capacitors pulsed into deep depletion by the clock phase voltages. For times much shorter than that required to form an inversion layer of minority carriers by thermal generation, potential wells will be formed at the silicon surface. The minority carrier charge representing the information will be stored or confined in these potential wells. The propagation of the information is accomplished by clock pulses applied to the electrodes of the successive MOS capac-



itors (i.e., charge-coupled elements), resulting in motion or spilling of charges from the potential wells that become shallower to the potential wells that become deeper. Such propagation of signal into successive minima of the surface potential produces a shift register for analog signals having signal transfer efficiency approaching unity. Such analog shift registers may be used for various signal processing applications such as electronically variable delays or self-scanning photosensor arrays.

### 1. Multi-Phase Charge-Coupled Devices

If the charge-coupled structures are formed with symmetrical potential wells, at least three phases are required to determine the direction of the signal flow. The use of more than three phases may be dictated by either the construction design symmetry, as in the case of a four-phase silicon gate overlapped by aluminum structures, or special signal coding schemes in which more than one bit may be propagated in one clock cycle. One important feature of the three-phase system is that it may be used for a bidirectional charge-coupled channel in which the flow of information may be reversed by reversing the timing of two of the three phase clocks.

### 2. Two-Phase Operation

Two-phase operation requires that the charge-coupled structures be formed so that the potential wells induced by the phase voltage pulses are deeper in the direction of the



signal flow. In this case, as one phase voltage is lowered, the resulting potential barriers force a unidirectional signal flow. It should be noted that a one-clock operation can also be obtained in a two-phase charge-coupled shift register if a proper dc voltage is applied to one of the phases [Ref. 2]. Furthermore, a true single-phase or a uniphase charge-coupled structure [Ref. 3] can be formed by replacing the dc-biased phase with a structure involving a fixed charge in the oxide.

## B. ANALOG SIGNAL PROCESSING APPLICATIONS

Greatly overshadowed, until recently, by imager development, analog signal processing is a fertile area for charge-coupled devices. Electronically variable analog delay lines, correlators, transversal filters and recursive filters are among the possibilities. It is assumed in all of these applications that the process is linear, that the technique of superposition applies to the input-output relationships. It is this assumption, or at least the linearity of charge-coupled devices, that is examined in this study.

### 1. Transversal Filters

Filters using the variable delay function of the charge-coupled device without employing signal feedback are classified as transversal filters. These filters are characterized by a finite memory and little or no phase distortion. Sharp cutoff in such a filter can only be achieved with a large number of terms, or delays, requiring many delay units to be fabricated. Such filters inherently require big charge-



coupled device arrays.

## 2. Recursive Filters

Recursive filters employ negative feedback of the output of the circuit to the input. Such filters enjoy infinite memory and use fewer terms than do transversal filters. The economy of terms, and hence delay lines, usually results in poor phase characteristics. It is simpler to obtain sharp cutoff using recursive techniques than with transversal. This represents an economy in charge-coupled structures required.

## 3. Variable Delay Lines

Since the charge-coupled device moves signals along the surface of a channel beneath clocking gates, it is the frequency of the clocking signal and the number of charge-coupled elements that determine the delay to which a signal is subjected. Variation of the clocking frequency can be easily achieved. Such variation permits simple electronic control of the delay provided by the device. Use of low clocking frequencies provides the capability for small long time delay units, as well as providing a fine tuning capability.



## II. NATURE OF PROBLEM

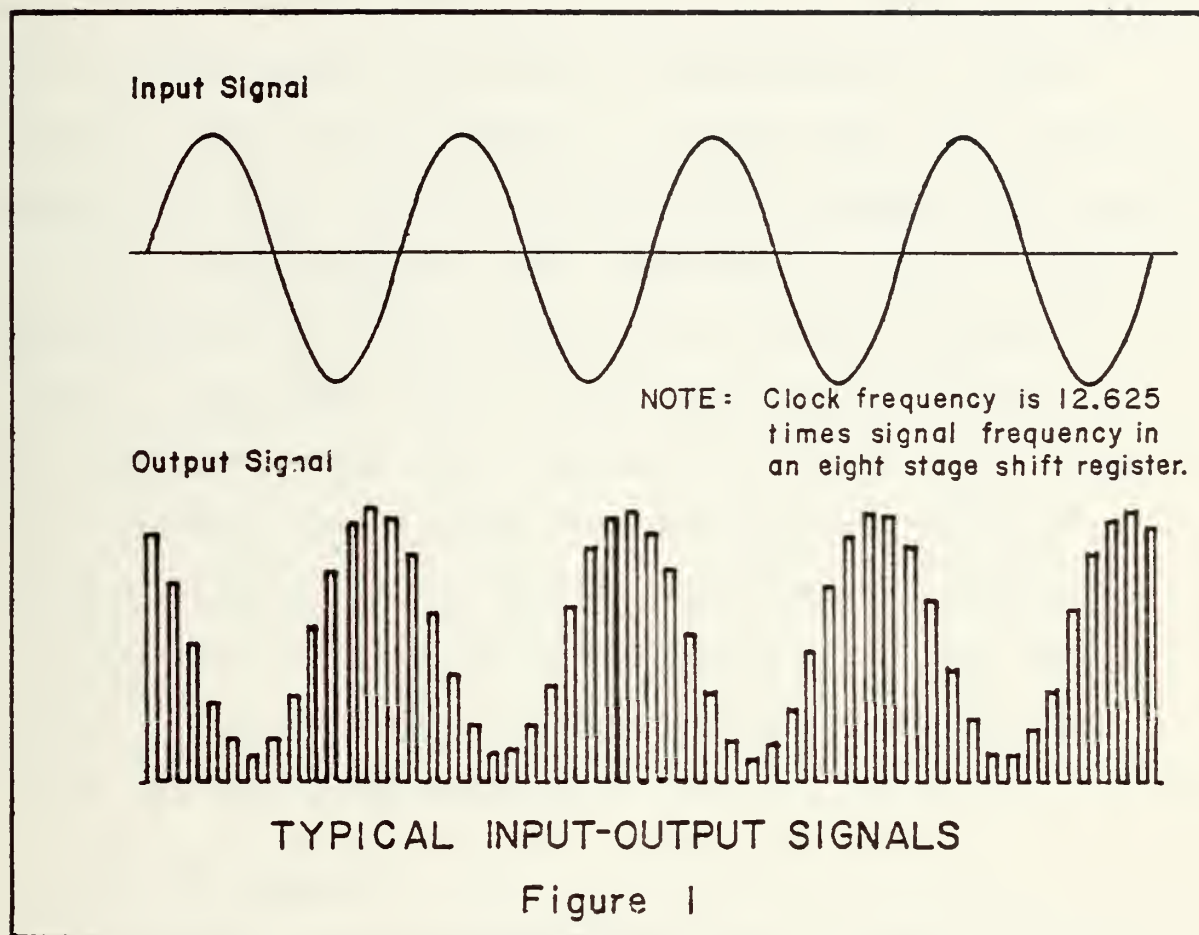
The principle of superposition is so pervasive in the area of analog signal processing that nearly all circuit design and analysis is dependent upon the linear nature of the components used. Specifically, in the design of both transversal and recursive filters, the process is assumed to be linear as a fundamental concept. In analog signal processing, it is vital that the charge-coupled device be operated in such a manner that the assumption of linearity be valid. How to assure linear operation is the nature of the problem.

### A. SAMPLED NATURE OF THE OUTPUT

In charge-coupled devices, an output signal is only available when the clock phases have moved a quantity of charge to the output of the device. This quantity of charge may be proportional to an input signal level present at the input of the device at a time in the past equal to the number of charge-coupled structures divided by twice the clocking frequency. The output of the device appears as a sampled version of the input waveform delayed in time as shown in Figure 1. The sample rate and the delay time are set by the clock frequency. While a sampled output signal can hardly be considered linear; provided that the clock frequency is high relative to the signal frequency, the linear nature may be easily provided by the use of a sample and hold circuit, or



in some cases by a low pass filter.



#### B. ESTABLISHMENT OF THE OPERATING POINT

The experimental devices used in this study required the setting of ten variables for operation. In most cases, these variables were tuned for operation only. The establishment of an operating point for linear operation was primarily a function of the dc-bias levels placed on the input ports of the device. The absolute level of these biases was effected by some of the other parameters, but the relative value of one to the others established the linear region desired. An extensive part of this study was the determination of the bias levels necessary for linear operation.



### C. TWO-PORT MODEL

When electronic devices are operated so that non-linear distortion is small, they can be approximated by linear equations and circuit elements. In such cases, all the procedures of linear circuit analysis may be applied and complex circuits may be analyzed with a minimum of effort. Such an approximation is a linear model or equivalent circuit of the device. This model can be used to determine the effect of the electronic device on an external circuit. It is important to realize that a model does not represent the actual internal behavior of the device. Most active devices used in electronic circuits may be modeled as a two-port linear system. It is reasonable to assume that a charge-coupled device may also be so modeled.

### D. OUTPUT LINEARITY

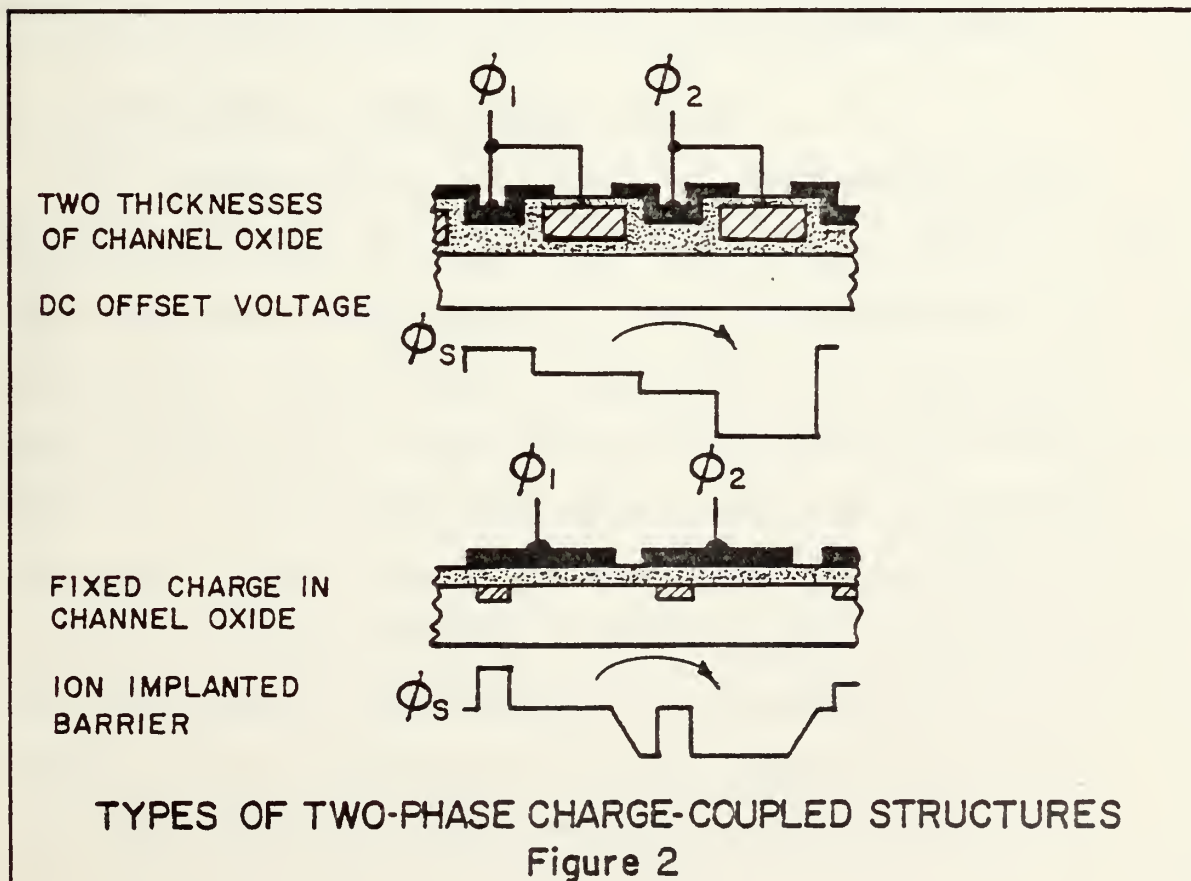
The representation of the signal by a quantity of charge in a potential well within the semiconductor produces a high impedance sensing problem. The output circuitry must provide for sensing the quantity of charge on each sampling by the clock phase, provide power to the succeeding circuits without diminishing the signal charge, and finally, it must discard the remnants of the signal charge after sampling. If the device is to be linear, then this output circuit must also be linear.



### III. TWO-PHASE CHARGE-COUPLED SHIFT REGISTER

#### A. TYPES OF TWO-PHASE CCD'S

The charge-coupled devices initially described by Boyle and Smith [Ref. 1] require three or more phase clocks to obtain directionality of signal flow. However, for most applications, high packing density and better performance may be achieved with two-phase charge-coupled structures. As illustrated in Figure 2, the asymmetrical potential wells or barriers in the surface potential, needed to provide directionality of the information flow for the two-phase operation can be achieved by incorporating into the charge-coupled structures one of the fol-





lowing features:

1. two thicknesses of the channel oxide,
2. dc offset voltage between two adjacent gates powered by the same phase voltage,
3. two levels of fixed charge in the channel oxide, or
4. ion-implanted barriers.

The first three of the above two-phase charge-coupled shift registers can be conveniently implemented by self-aligned, closely spaced structures in the form of polysilicon gates overlapped by aluminum gates [Ref. 4]. In the experimental part of this study, a charge-coupled device of the first type above was used. Described in this section in greater detail, it was a two-phase CCD with two thicknesses of channel oxide using polysilicon and aluminum gates.

## B. DESCRIPTION OF EXPERIMENTAL DEVICE

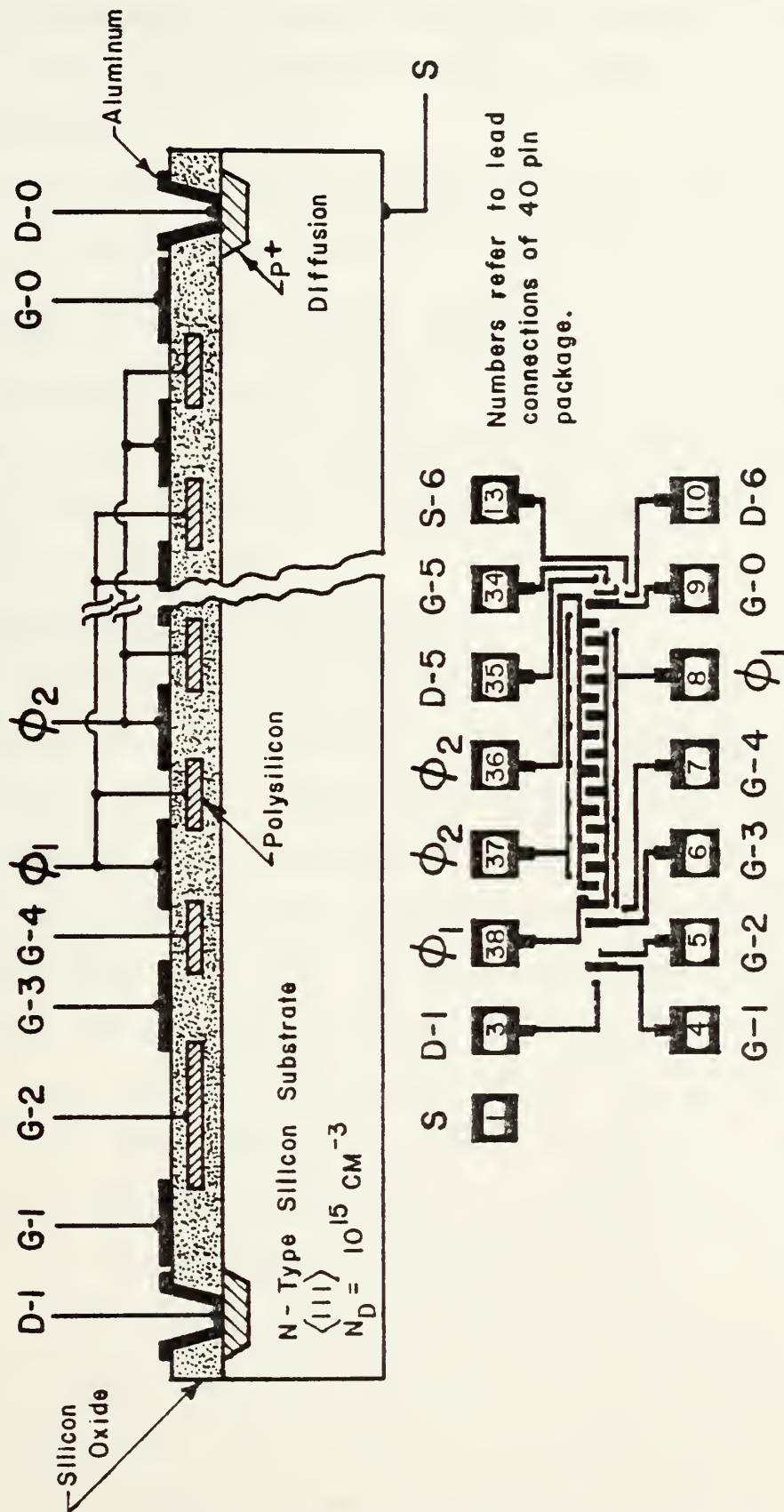
The device used in this study was fabricated by TRW, Incorporated, for the purpose of experimental studies. The substrate used was 1.5 ohm-cm., n-type silicon with <111> orientation. Construction of the device is illustrated in cross-section with a plan view of the final metallization in Figure 3. Six  $p^+$ -diffusions were inserted to act as input and output diodes, and as the source and drain diffusions for two output circuit MOSFETs. Thermally grown silicon dioxide,  $SiO_2$ , was grown to approximately 1000 Angstrom ( $\text{\AA}$ ) to act as channel oxide. Polysilicon film was deposited and defined into the polysilicon gates. A second layer of silicon



dioxide was thermally grown for the aluminum gates to a total thickness of 3000 Å. The device structure was completed by opening contacts through the silicon dioxide to the  $p^+$ -diffusions and the polysilicon gates. A final metallization of aluminum was deposited and defined into gates, contact lands and leads. The entire structure was approximately 33 mils long by 14 mils wide. The shift register input gates consisted of two aluminum gates and a polysilicon gate, each 0.5 mils long by 2.0 mils wide, and a polysilicon gate, 1.5 mils long by 2.0 mils wide. The channel gates were each 0.5 mils long by 2.0 mils wide, resulting in a channel length of 2.0 mils per shift register stage. The output gate was 0.5 mils long by 2.0 mils wide. The two MOSFETs were 0.6 mils long by 0.4 mils wide.

As shown in Figure 3, the device had an input stage consisting of the source or input diode, D-1, the input gates, G-1, G-2, G-3 and G-4. Separate electrical access had also been provided to the polysilicon and aluminum electrodes of each phase; i.e.,  $\phi$ -1 (polysilicon),  $\phi$ -1 (aluminum),  $\phi$ -2 (polysilicon), and  $\phi$ -2 (aluminum). The output was sensed as a current flow out of the source diffusion or output diode, D-0. The output gate, G-0, provided a means of setting the surface potential in the vicinity of the output diode. Two MOSFETs were diffused onto the substrate, with one having its gate and drain available for connection, G-5 and D-5. The other MOSFET had its drain and source available as D-6 and S-6. The second MOSFET gate, the source of the other





Cross-sectional view and plan of 8-stage shift register used.

Figure 3



MOSFET and the output diode were connected together on the substrate, but were not available off the substrate for external connection.

The device was mounted in a forty lead flat pack, but was not sealed or protected against the environment.

## C. OPERATION OF THE EXPERIMENTAL DEVICE

The experimental device used in this study was a two-phase charge-coupled shift register employing two thicknesses of channel oxide to achieve the asymmetrical potential wells necessary for signal flow.

### 1. Charge-Transfer Operations

Assuming essentially zero fixed charge in the channel oxide, substrates with relatively large doping concentrations are required to obtain a substantial difference between the surface potential under the polysilicon gates and the potential under the aluminum gates powered by the same phase voltage. It has been found [Ref. 5] that the potential barrier formed under the aluminum gate with respect to the surface potential under the polysilicon gate of the same phase is not constant as the phase voltage changes. The maximum amount of charge signal that can be stored and transferred depends in some degree on the frequency and the waveshapes of the phase voltages. These waveshapes may be symmetrical with equal rise time and fall time, nonoverlapping, or overlapping. In the overlapping case, the transfer of charge is preceded by the condition in which both phase voltages are minimum. If it is assumed that the signal charge is originally contained

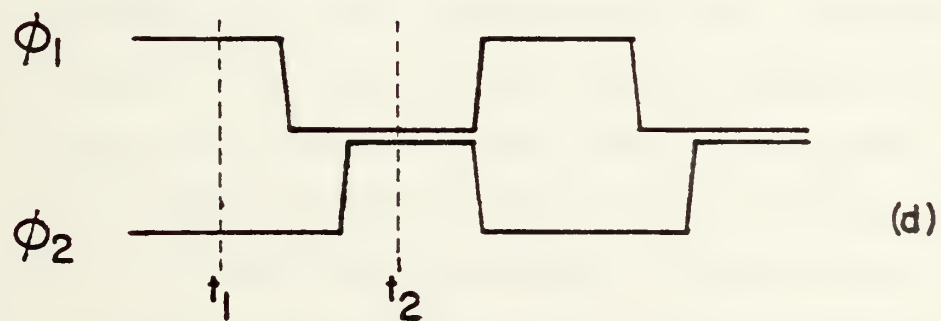
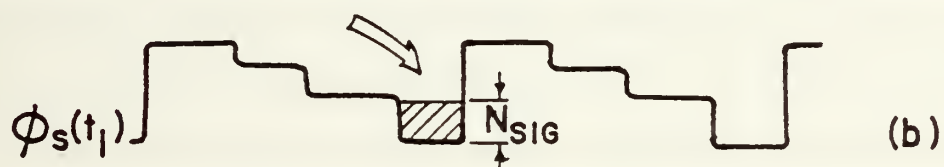
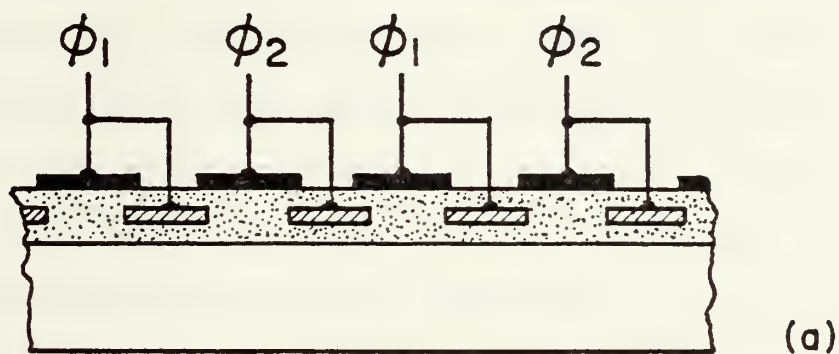


in the potential well beneath the phase-one gate, then as the phase voltage,  $V_{\phi_1}$  is changed from  $V_{\phi_1} = -23$  volts to  $V_{\phi_1} = -13$  volts, the surface potential under the phase-one gate is raised to a higher value, the charge signal is transferred to the potential well under the phase-two gate. This mode of operation for two-phase charge-coupled devices may be referred to as the "complete charge-transfer" mode.

The experimental device used in this study was operated in the complete charge-transfer mode using overlapping wave-shapes with near equal rise and fall times for the two phase voltages. This complete charge-transfer mode of operation is illustrated in Figure 4 by two profiles of the surface potential. In this case, at time  $t_1$ , the charge signal is accumulating in the potential wells under the phase-two gates; and in the second half-cycle, at time  $t_2$ , the charge signal will be transferred to the potential wells under the phase-one gates.

Another mode of operation of two-phase charge-coupled devices can be achieved if the surface potential under the aluminum gates is maintained high enough in all cases so that the potential wells under the polysilicon gates can never be completely emptied. In other words, the surface potential under the polysilicon gates powered by the minimum phase voltage is lower than the surface potential under the aluminum gates powered by the maximum phase voltage. This mode of operation may be considered the "bias charge" or "bucket-brigade" mode. A bias charge, or background charge will





Charge-transfer operation of the 2-phase CCD.

Figure 4



always be present under all the polysilicon gates in this mode. In steady-state operation, the bias charge will be maintained by thermal generation.

The transition from the complete charge-transfer mode to the bias-charge mode of operation could be accomplished by increasing the dc-bias level of the phase voltages. The presence of positive charge in the channel oxide, in the case of n-channel devices, will also increase the barriers under the aluminum gates sufficient to cause bucket-brigade mode of operation. The bias-charge mode of operation of two-phase charge-coupled shift registers is very similar to the operation of bucket-brigade [Ref. 6] shift registers. In the bucket-brigade device case, the bias charge regions are replaced by floating diffusions; otherwise, the operation of the two types of shift registers is very similar.

As was generally known in connection with the operation of a bucket-brigade shift register [Ref. 6], a two-phase charge-coupled shift register can also be operated with one of the phases dc-biased at a level used on the other phase. Since no switching levels are used on the dc phase, this is referred to as "one-phase" operation. This one-phase operation was confirmed with the experimental device used in this study.

A uniphase charge-coupled structure requiring only one set of externally controlled gates could be fabricated. Such a device would require that the dc-biased phase gate be



replaced by built-in bias in the structure. This bias may be obtained by the intentional presence of fixed charge in the channel oxide.

## 2. Signal Input to the Experimental Device

Many different techniques have been developed for the insertion of charge in charge-coupled shift registers. For use as an analog signal processing device, it is desirable that the technique used produce a charge quantity in the potential well of the charge-coupled shift register that is linearly related to the signal potential or current. Further, the technique should not inject noise and preferably should demonstrate high transfer efficiency.

In the device studied, charge injection by potential equilibrium or "sloshing" technique was used. This method of signal charge injection is demonstrated in Figure 5. This diagram shows the three sequential surface potential conditions that exist during one transfer cycle. Also shown are the relative voltage levels required to produce the diagrammed surface potentials at the times  $t_1$ ,  $t_2$  and  $t_3$ . The input diode is pulsed to a low potential,  $V_{DI}$ , to inject charge into the potential wells formed under the input gates G1, G2, G3 and G4. The quantity of charge injected is a function of the level to which the diode is forward biased, the duration of the pulse, and the depth of the potential wells under the input gates. It is limited by the magnitude of the input pulse and the potential barrier under the first phase gate. This condition is demonstrated by the surface potential dia-

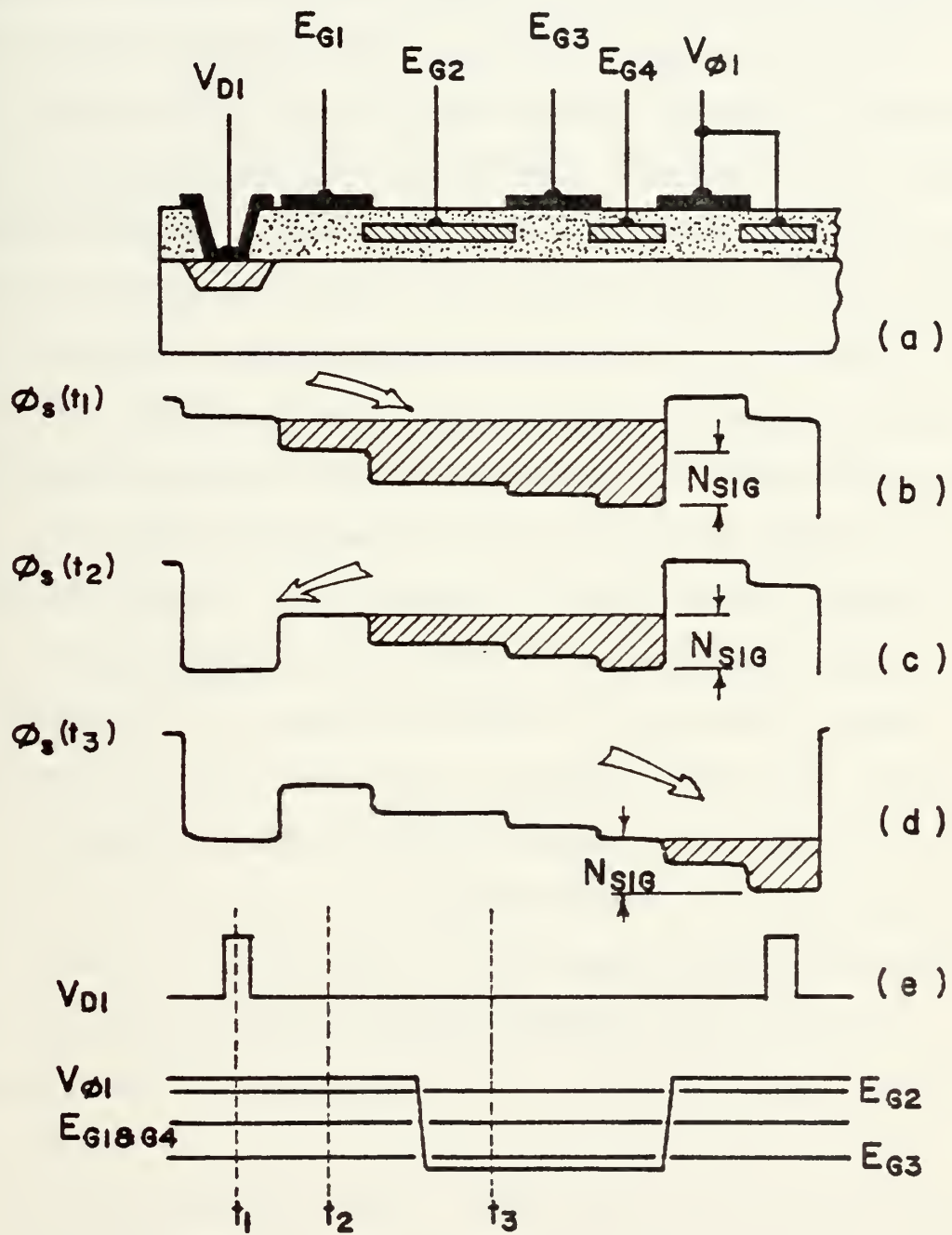


gram in Figure 5b, the condition existing at time  $t_1$ . At the end of the input pulse, the input diode is reverse biased. Excess charge in the potential wells under the input gates is drained through the reverse biased input diode. The charge level is set by the surface potential under the first input gate, G1, and the first clocking phase gate. The quantity of charge is established by the depths of the wells formed by the surface potentials under the input gates, G2, G3 and G4. This condition is shown in Figure 5c, existing at time  $t_2$ . Notice that, provided that the input pulse produced sufficient charge to fill the wells under the input gates, the signal charge is no longer a function of the input pulse. A major source of input non-linearity, the input diode, has been thus dispatched. Following the disposal of excess charge through the input diode, the first clocking gates are pulsed to a low potential by the clock voltage. Accumulated charge under the input gates is now transferred to the potential well under the first clocking gates. This condition is diagramed in Figure 5d, as the condition existing at time  $t_3$ . As can be seen, the input signal charge quantity is a function of the surface potentials beneath the input gates. The determination of the signal levels for which a linear input can be obtained was a very large portion of this study.

### 3. Output Circuit Used in the Study

The output circuit used in the experimental study employed an output diode, a reset MOSFET, and an output MOSFET connected as a source follower. The circuit schematic is





Charge input operation.

Figure 5



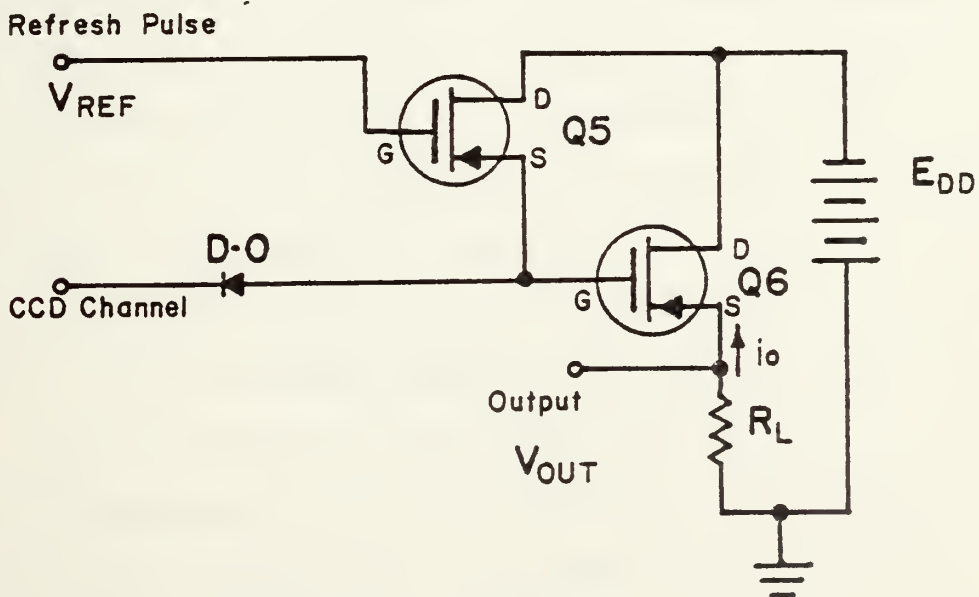
shown in Figure 6. The output diode, DO, is reverse biased by the drain bias voltage,  $E_{DD}$ , through the reset transistor, Q5. The degree of reverse bias is determined by the surface potential adjacent to the diode diffusion in the charge-coupled device channel. This surface potential is set by a dc-bias on an output gate not shown in the diagram. This output gate is an aluminum gate immediately adjacent to the output diode diffusion. This output gate could be connected to the phase clock voltage of the gates next to it, but experimentally, better noise immunity was obtained with a dc-bias. When the phase clocked gates at the end of the charge-coupled structure are sent to their low potential, the surface potential well developed beneath them accepts the signal charge of minority carriers. The presence of this signal charge modifies the potential at the cathode of the output diode. Since the charge in the depletion layer of the diode is bound, the potential at the anode rises to reflect the signal charge. The increasing potential at the anode of the output diode is applied to the gate of the output MOSFET, Q6. The more positive potential at the gate of the output MOSFET decreases the drain to source current flowing through this transistor. The lessened drain current results in a more positive voltage at the output.

At the completion of the clock phase cycle which opened the clocking gates at the end of the shift register, the surface potential barrier again blocks the transfer of charge signal to the output diode. A refreshing pulse is applied



to the heretofore cutoff reset MOSFET, Q5. This negative going refresh pulse turns Q5 on and restores the output diode to a fully reverse biased condition; sets the quiescent voltage on the gate of the output MOSFET, Q6, at or near the value of the drain bias supply; and provides a low impedance path for the previous signal charge to flow to ground through the reverse biased output diode.

This output circuit permitted isolation of the small charge packets that represented samples of the input signal from the loading effects of the electronic test instrumentation that was used in the study. The linearity, that is the relationship between the potential produced by the charge signal at the cathode of the output diode and the voltage output of the source follower, of this circuit will be analyzed further in another section of this study.



OUTPUT CIRCUIT  
Figure 6



#### IV. EXPERIMENTAL PROCEDURES

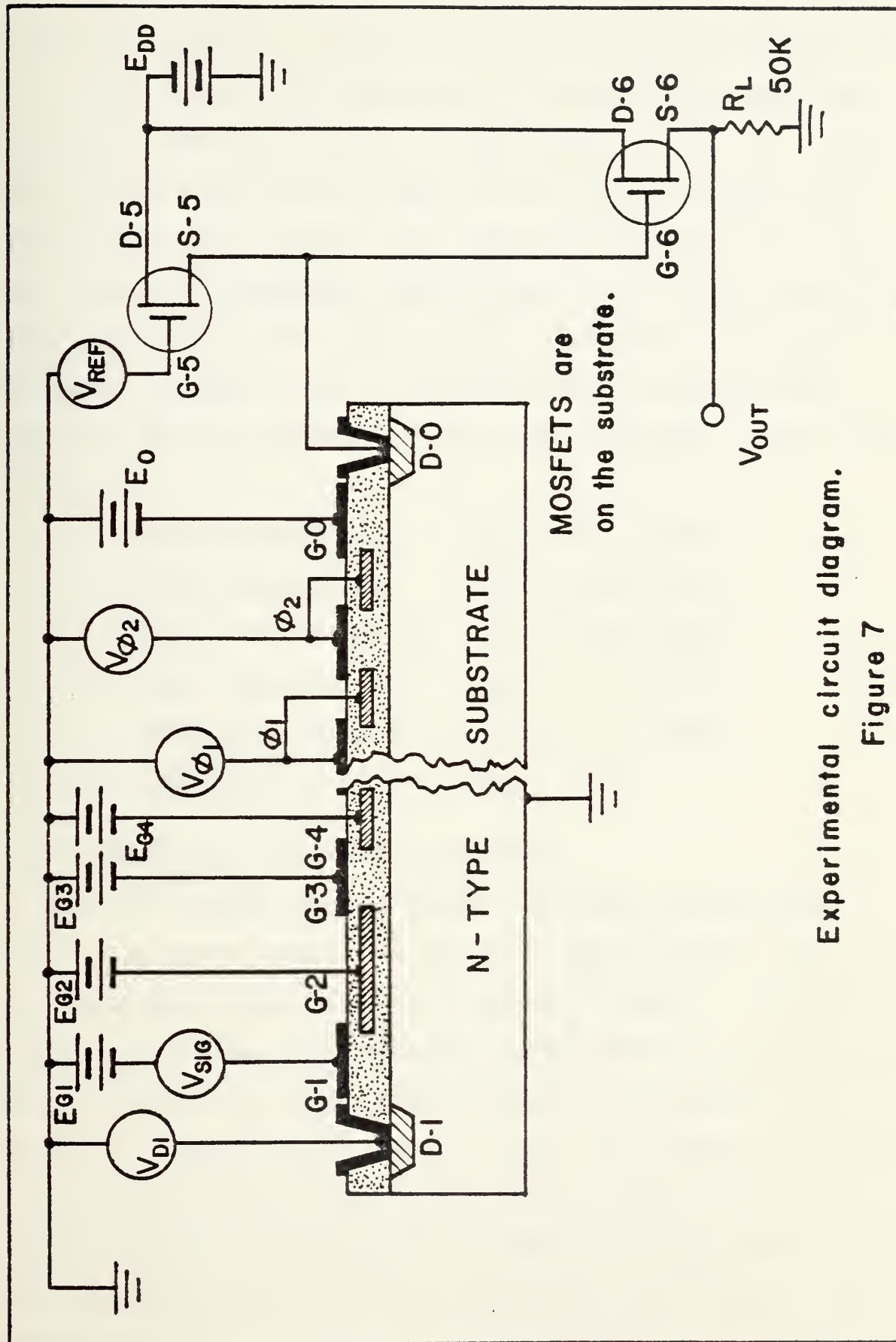
The experimental study of the two-phase charge-coupled shift register reported in this paper evolved into six areas:

1. To accomplish charge transfer,
2. To establish linear signal transfer,
3. To determine the device gain,
4. To determine circuit model parameters,
5. To establish linear operating regions, and
6. To determine the characteristics of the output MOSFET.

##### A. TO ACCOMPLISH CHARGE TRANSFER

The experimental device was connected as shown in Figure 7. Using parameter values provided by the manufacturer based on a computer study of a typical device, charge transfer was established by trial and error. As a general technique, dc-bias levels were applied to the input gates, G1, G2, G3 and G4. Since no data was available on the surface potential-gate voltage relationship of these gates, these levels were determined empirically and usually were found to be the most critical of all parameters effecting the performance of the device. The potential on the output gate,  $E_0$ , was set at a previously successful value of -30 volts. The MOSFET drain-bias,  $E_{DD}$ , was likewise set at a nominal value of -25 volts. The clocking phase voltages were set at the manufacturer's





Experimental circuit diagram.

Figure 7



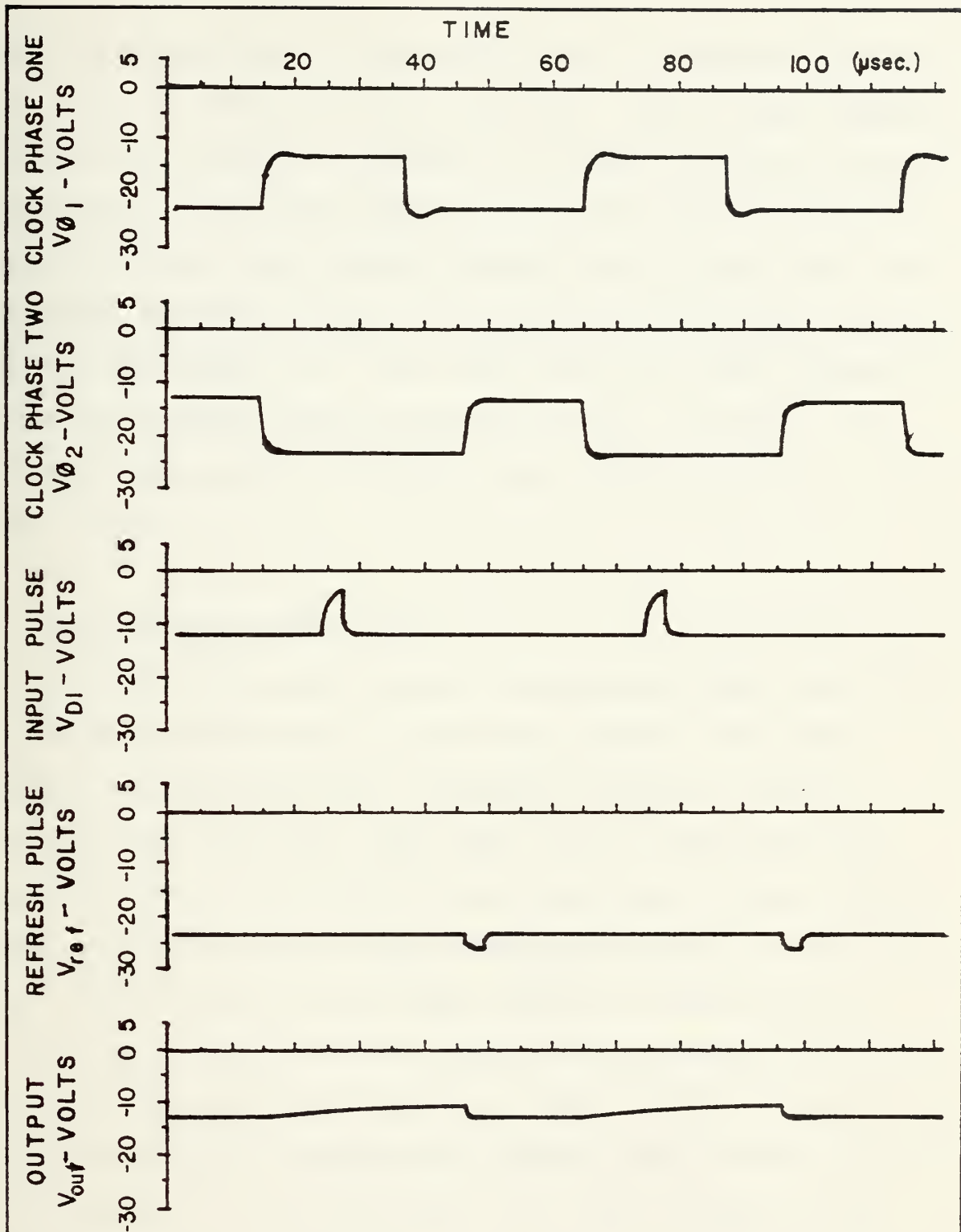
recommended values. The dc-bias level and pulse amplitude of the refresh pulse,  $V_{\text{ref}}$ , were set to a value that would turn the reset MOSFET off and on (pulsing from +2 to -1 volts relative to the drain bias). The dc level and pulse amplitude of the input diode supply,  $V_{\text{DI}}$ , was then adjusted until signals could be observed by oscilloscope at the output terminal. Minor perturbations were made on all parameters to maximize the output current pulses. A typical set of operating waveforms are shown in Figure 8. For these waveforms, the dc-bias levels were:

1. MOSFET Drain Bias,  $E_{\text{DD}} = -25.0$  volts
2. Output Gate Bias,  $E_0 = -30.0$  volts
3. Input Gate One Bias,  $E_{\text{G1}} = -19.6$  volts
4. Input Gate Two Bias,  $E_{\text{G2}} = -20.0$  volts
5. Input Gate Three Bias,  $E_{\text{G3}} = -22.0$  volts
6. Input Gate Four Bias,  $E_{\text{G4}} = V_{\phi 1}$

#### B. TO ESTABLISH LINEAR SIGNAL TRANSFER

With the charge-coupled device providing signal charge transfer as above without an external signal applied, the input diode pulse amplitude was increased slightly. If the output pulses showed no increase in amplitude, then potential equilibrium input had been obtained...the signal level was not a function of the input diode pulse. Should this not occur, the input gate biases were modified until potential equilibrium input was obtained. A small ac-signal level was then impressed upon any of the input gates for testing. The





TYPICAL PROCESSING WAVEFORMS

Figure 8



device parameters were then again tuned to optimize the signal output for amplitude and linearity. With a small signal, linearity was usually optimized by slightly varying the dc-bias level of the input signal so that the output quiescent value of voltage lay halfway between the no signal level and the fully saturated output. The phase shift between the input and the output, i.e., the time delay, was then checked to insure that shift register action had been obtained. The observed delay was to be eight times the period of the clocking voltage.

#### C. TO DETERMINE DEVICE GAIN

Once the device was set into an operating mode, two techniques were established for gain measurement. The first termed dc-gain measurement, involved setting the dc-bias values on all the input gates save one at independent parametric values. The dc-bias on the remaining, or now, signal, input gate was varied at small voltage intervals. The resulting source current of the output MOSFET was determined and plotted as a function of the input gate potential. The second technique involved inserting a small, known, ac signal on the input gate and measuring the output signal either with an oscilloscope or a wave analyzer. The small signal ac-gain thus determined by the ratio of these ac values or from the slope of the plot of the first technique was recorded as the gain. In the actual case, the first technique was used to the exclusion of the second except for spot checks of results.



Use of the peak pulse output current as a function of the input signal voltage permitted a more precise determination of the device gain. The slope of this plot multiplied by the value of the output resistance yielded the small signal voltage gain.

A minicomputer, an instrument/computer interface unit and two digital multimeters were used for semiautomatic data collection. The equipment employed was:

Minicomputer, TEKTRONIX Model 31

Calculator-Instrument Interface, TEKTRONIX 153

Digital Multimeter, TEKTRONIX DM 501

One voltmeter was connected across the device output and the other was connected to the selected input gate. A series of calibration runs were conducted to determine the peak output pulse current as a function of the output voltage read on the digital voltmeter. The slope of this curve provided a proportionality constant for converting the dc voltage read on the digital meter to a peak pulse current value. An extremely low frequency function generator was connected to the selected input gate as the signal source. A ramp function at a frequency of about 0.002 Hz was used to vary the input gate signal at such a rate that the input voltage would change by only the least significant digit of interest in one sample period of the digital voltmeter. The computer, which sampled both the input and output voltmeters, was programmed to store both voltages read at the instant that the input voltage was equal to a comparison value stored in the comput-



er. When the read condition had been satisfied and the data stored, the comparison value would be incremented by the delta value inserted previously by the operator. The computer would then again wait for a matching condition. In such a manner, it was possible to automatically record the input and output voltages for as many values as the operator designated at the start of a run, commencing at a given input voltage and incremented by a given change of input. After the desired number of data points had been recorded, the computer would print out the values of the input voltage and the product of the output voltage and the previously determined proportionality constant, i.e., the output peak pulse current.

As inputs to the semiautomatic routine, the operator need only type in:

1. An arbitrary run number,
2. Initial input voltage,
3. Desired incremental increase in input voltage,
4. The number of input data points desired, and
5. The proportionality constant to convert output

dc voltage to peak pulse source current.

The operator would then start the function generator at some value of output less than the initial input voltage selected at the frequency necessary to permit the voltage to change at a slow enough rate, and then pursue other investigations until the computer printed out the data.



#### D. TO DETERMINE CIRCUIT MODEL PARAMETERS

Initially, in the study, it was felt that the charge-coupled shift register could be modeled as a two-port linear device. To support such a model, considerable effort was expended in efforts to determine the input admittance, output impedance and transfer functions. In fact, none of the required parameters were successfully measured except for the gain as described above. The pulsed nature of the device, that is, the presence of a pulsed waveform at the output, even with no input signal present interfered with the determination of the output impedance. The many signals necessary to cause a CCD to function, even at a quiescent level, produced a need for many connections to the device. These connections terminated in several signal generators and power supplies. All efforts to measure the input admittance of the device were swamped by the background capacitance and noise of the experimental setup.

#### E. TO ESTABLISH LINEAR OPERATING REGIONS

With the multiple input gates, the possibility of using the charge-coupled shift register as an adder or subtractor of analog signals is obvious. A major requirement for such operations to be successful would be that the device be linear with respect to all signals inputted. It is thus necessary to know for what values of input voltages on all gates will linear operation result. The individual dc gain curves were evaluated to determine the regions over which operation



was linear. These curves showed a prompt departure from linearity at a high and a low value for whichever input gate was being used as the controlling gate. These departures occurred when the potential wells were nearly filled, saturation; and when the wells were nearly empty, that is the signal charges could not be sensed at the output.

#### F. TO DETERMINE THE CHARACTERISTICS OF THE OUTPUT MOSFET

At the request of the experimenter, the device manufacturer established the test connections shown in Figure 9 on the output MOSFET of four devices similar to those used in this study. Under such an experimental connection, the voltage between the gate and the drain,  $V_{GD}$ , is zero. With this potential difference at zero, the gate to source voltage,  $V_{GS}$  is equal to the drain to source voltage,  $V_{DS}$ . This is the simplest arrangement for testing a MOSFET, for the transistor is then in the saturation region. From the basic circuit theory developed about the Sah MOSFET model [Ref. 7], under conditions of saturation; that is, when:

$$|V_{GS} - V_T| \leq |V_{DS}|$$

then:

$$I_{DS} = - \left( \frac{\mu_p \epsilon_r \epsilon_o}{2t_{ox}} \right) \left( \frac{W}{L} \right) (V_{GS} - V_T)^2 \quad (1)$$

where:  $\mu_p$  = average surface mobility of holes in the channel

$t_{ox}$  = thickness of the oxide over the channel

$\epsilon_r$  = relative permittivity of the oxide

$\epsilon_o$  = permittivity of free space,  $8.854 \times 10^{-14}$  farad/cm



$\ell$  = length of the channel in the direction of current flow

$W$  = width of the channel

$V_{GS}$  = gate to source voltage

$V_{DS}$  = drain to source voltage

$V_T$  = threshold voltage

Collecting some of the more or less constant terms from the above expression (1), permits the definition of two new constants:

$$k' = \frac{\mu_p \epsilon_r \epsilon_o}{2t_{ox}} \quad (2)$$

and,

$$k = k' \frac{W}{\ell} \quad (3)$$

Use of these new consolidated constants permits a simplification of the expression for the source-drain current to:

$$I_{DS} = -k(V_{GS} - V_T)^2 \quad (4)$$

Note that the parameter,  $k$ , is a design variable which is a function of the ratio of the channel width,  $W$ , and of the length of the channel in the direction of current flow,  $\ell$ . The parameter  $k'$  is fixed by the fabrication process. For purposes of nomenclature,  $k$  is described as the gain parameter, and  $k'$  is termed the conduction factor.

Using the same transistor model, the drain to source current in the non-saturation condition becomes:

$$I_{DS} = -k[2(V_{GS} - V_T)V_{DS} - (V_{DS})^2] \quad (5)$$

when:

$$|V_{GS} - V_T| > |V_{DS}|$$

In the saturation condition depicted in Figure 9, if drain to source resistance is neglected, a plot of  $|\sqrt{I_{DS}}|$

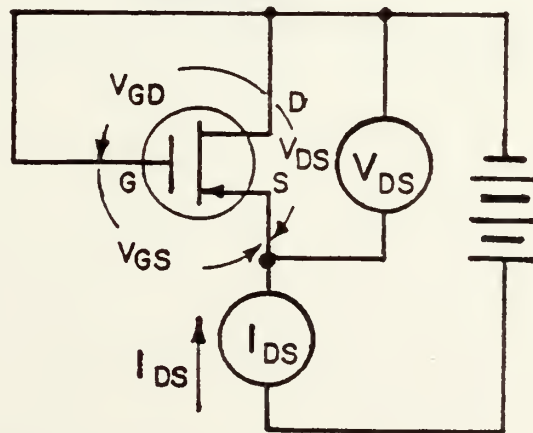


as a function of  $|V_{GS}|$ , (or  $V_{DS}$  since the two potentials are equal in this configuration) yields a straight line. The slope of this curve is  $\sqrt{k}$ , with an abscissa intercept of  $|V_T|$ . That this is so, may be quickly established by taking the square root of both sides of the equation expressing the drain-source current relationship to the gate-source voltage in saturation (1):

$$\sqrt{I_{DS}} = \sqrt{k} (V_{GS} - V_T) \quad (6)$$

Such a relationship is demonstrated in Figure 10.

The experimental device manufacturer provided the source to drain current and source to drain voltage data for ten data points on four samples of the output MOSFET.



**MOSFET TEST SETUP**

**Figure 9**



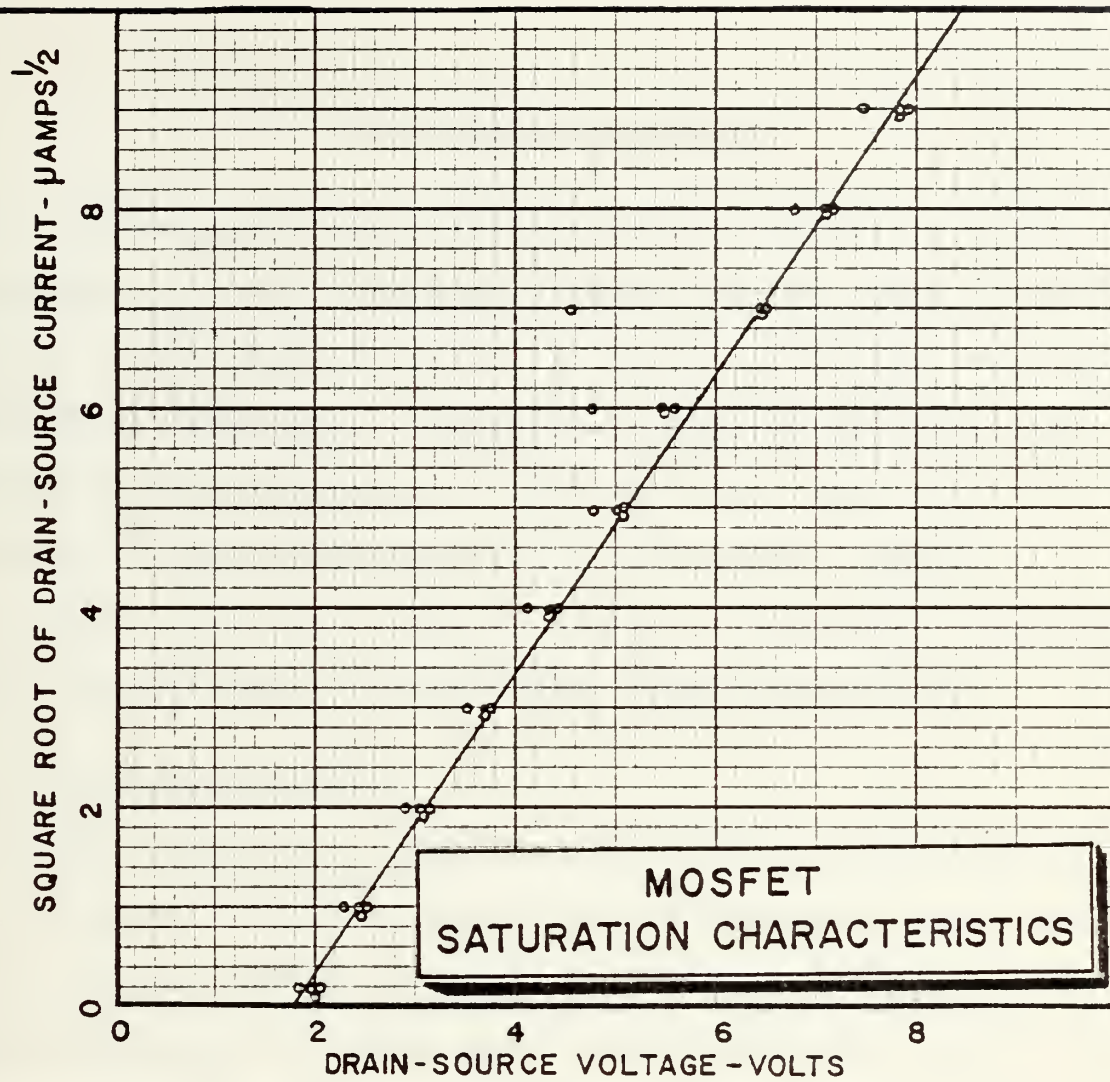


Figure 10



## V. PRESENTATION OF DATA

In reviewing the data obtained in this study, it should be remembered that it represents determinations made on three devices of the same design; and as near as possible, the same fabrication techniques. During the course of the study, no effort was made to produce a modified device that would be optimized to the conditions of the experiment. Rather, a stock device for basic study of charge-coupled shift register principles was used to study analog signal processing.

### A. DC GAIN MEASUREMENTS

DC gain determinations and output current pulse amplitude as a function of control gate voltage measurements were made for thirty-six variations of the independent parameters. In these measurements, control gate 4 was connected to the clocking signal for phase one, thus becoming part of the clocking structure. The voltage on control gate one was varied as the independent variable. The peak pulse current amplitude of the output signal pulse was defined as the dependent variable. The dc potentials, or biases, on control gates 2 and 3 were set as independent parameters. The functional relationship demonstrated in Figure 11 is typical of the data obtained. From such data, the device gain can be obtained by multiplying the slope of the curve times the output load resistance, as:

$$g = \frac{dI}{dV} R_L \quad (7)$$



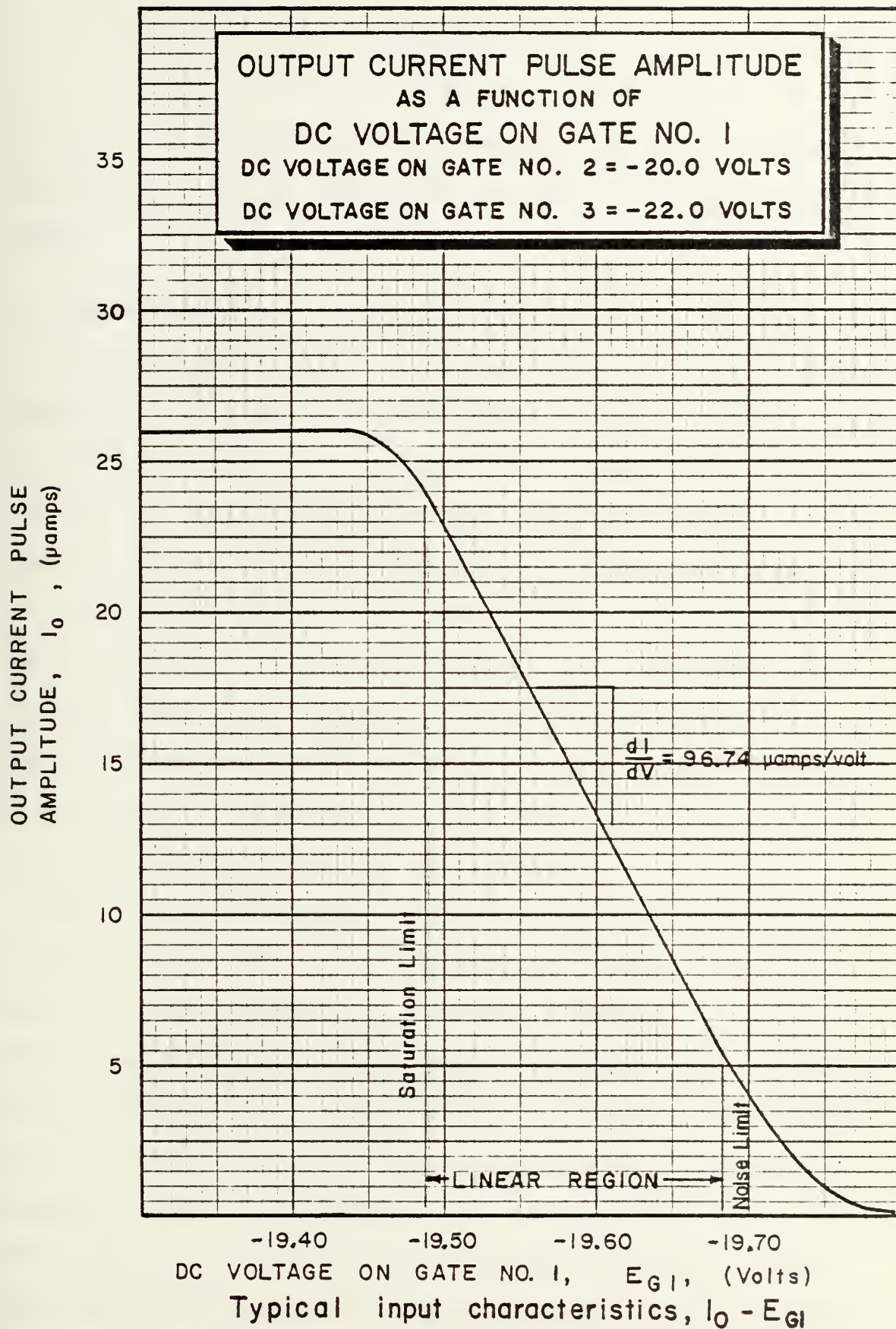


Figure II



$$\text{or } g = 96.74 \times 10^{-6} \times 50 \times 10^3$$

$$g = 4.8$$

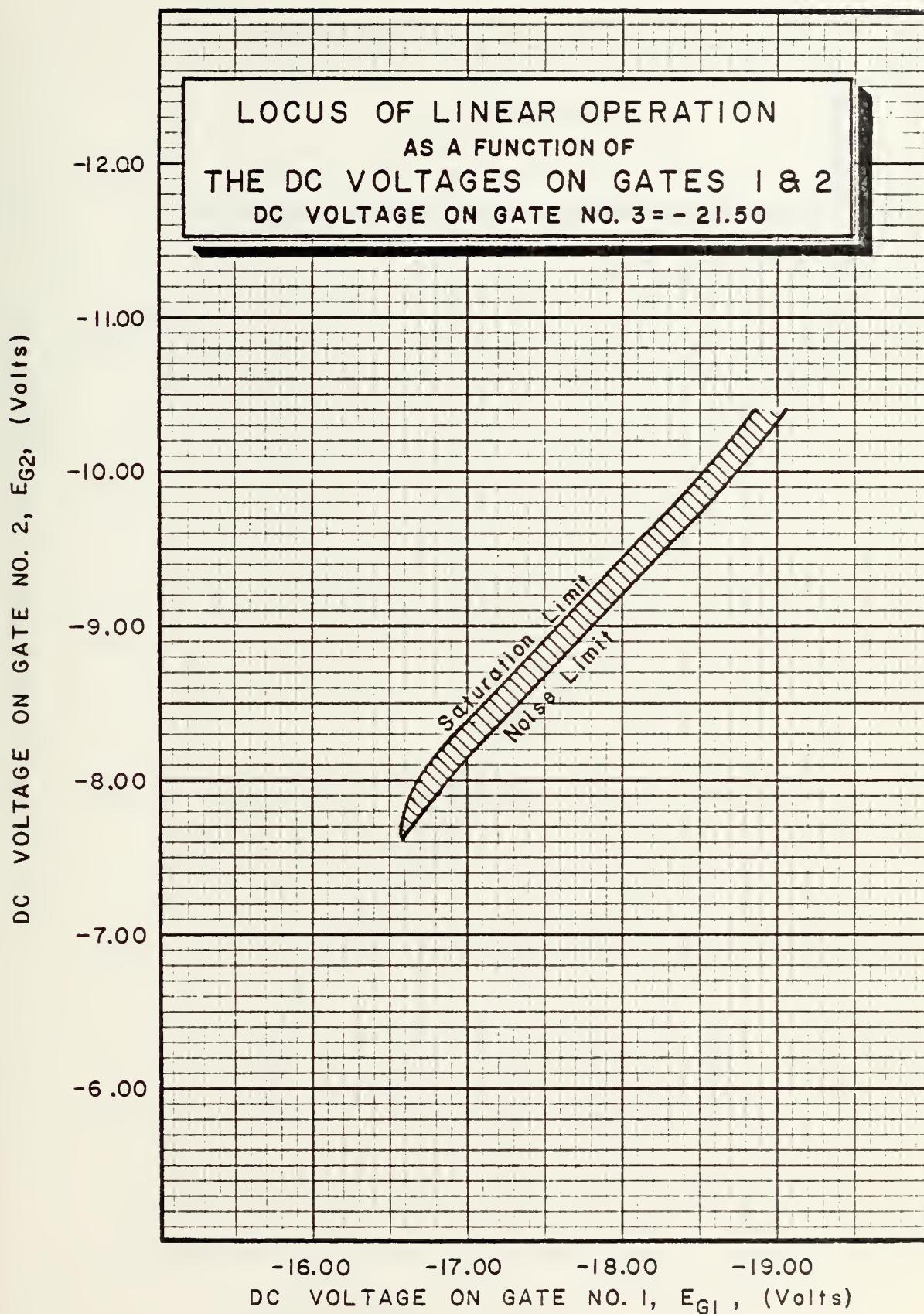
A gain of 4.8 was observed over most of the useful range of input signal. At the limits of operability, the gain was reduced.

## B. LINEAR REGIONS

In the DC gain studies, there were two independent parameters, the voltages on control gates 2 and 3. Since adjustment of these parameters changed the voltage range of control gate one over which the output was linearly related to the input, it seemed that a second gate could be used to permit a dual input. In such an arrangement, input signals could be applied to gates one and two, or gates one and three. No study was made to determine the relationship of inputs on gates two and three, or for inputs on three or more gates at the same time. The capability to respond to inputs on more than two gates certainly exists, however.

The DC gain curves were studied to determine at what voltages on gate one departure from linearity would occur as a function of the voltages on gates two and three. This parametric study provided the regions over which linear operation could be achieved as a function of the voltage on two control gates with the voltage on the third gate as an independent parameter. The resulting loci of linear operation are presented in Figures 12 and 13. The range of voltage used on control gate one was kept the same for the study of the effect of control gate two and the effect of control gate three. As

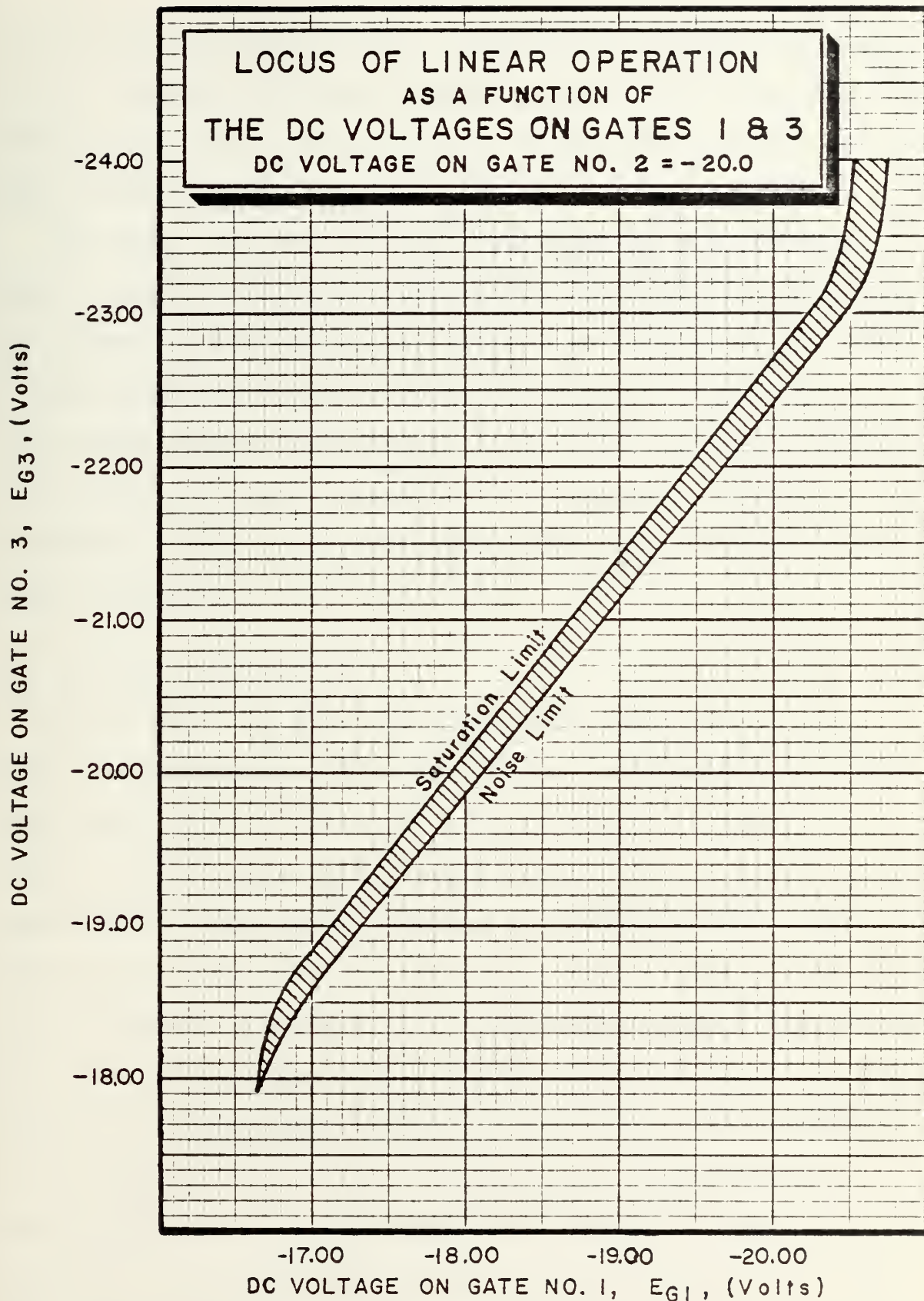




Locus of linear operation, gates 1 and 2.

Figure 12





Locus of linear operation, gates 1 and 3.

Figure 13



can be seen from the two loci, simultaneous linear operation can be achieved for signals on two gates. It should be noted, however, that the dynamic range of simultaneous inputs is small, approximately 0.1 to 0.2 volts.

The upper limits of the loci were not defined in this study. This was because linear operation could be continued with proper adjustment of the various potentials on the CCD as the signals became more and more negative. The limit of such accommodation would appear to be the breakdown potential of the various gates concerned. A "saturation" effect of the potential on gate one can be seen in the upper limits of Figure 13, however.

#### C. AC GAIN CONFIRMATION

Small signal AC gain determinations were made on the device to confirm the DC measurements. A 20 millivolt (rms) signal was applied to control gate one with all other input gates at bias levels equivalent to those used in the DC gain measurements. The output voltage was measured with a wave analyzer, and the ratio of the output rms voltage at the signal fundamental frequency to the input rms voltage was recorded as the voltage gain. The dc-bias on control gate one was varied as an independent parameter and the AC gain determined as a function of this bias. Figure 14 is representative of the results obtained. No significant departure from this curve was noted by varying the input signal frequency. The gain level of 4.75 observed agrees well with the 4.8 from the DC gain determinations. A horizontal translation of the



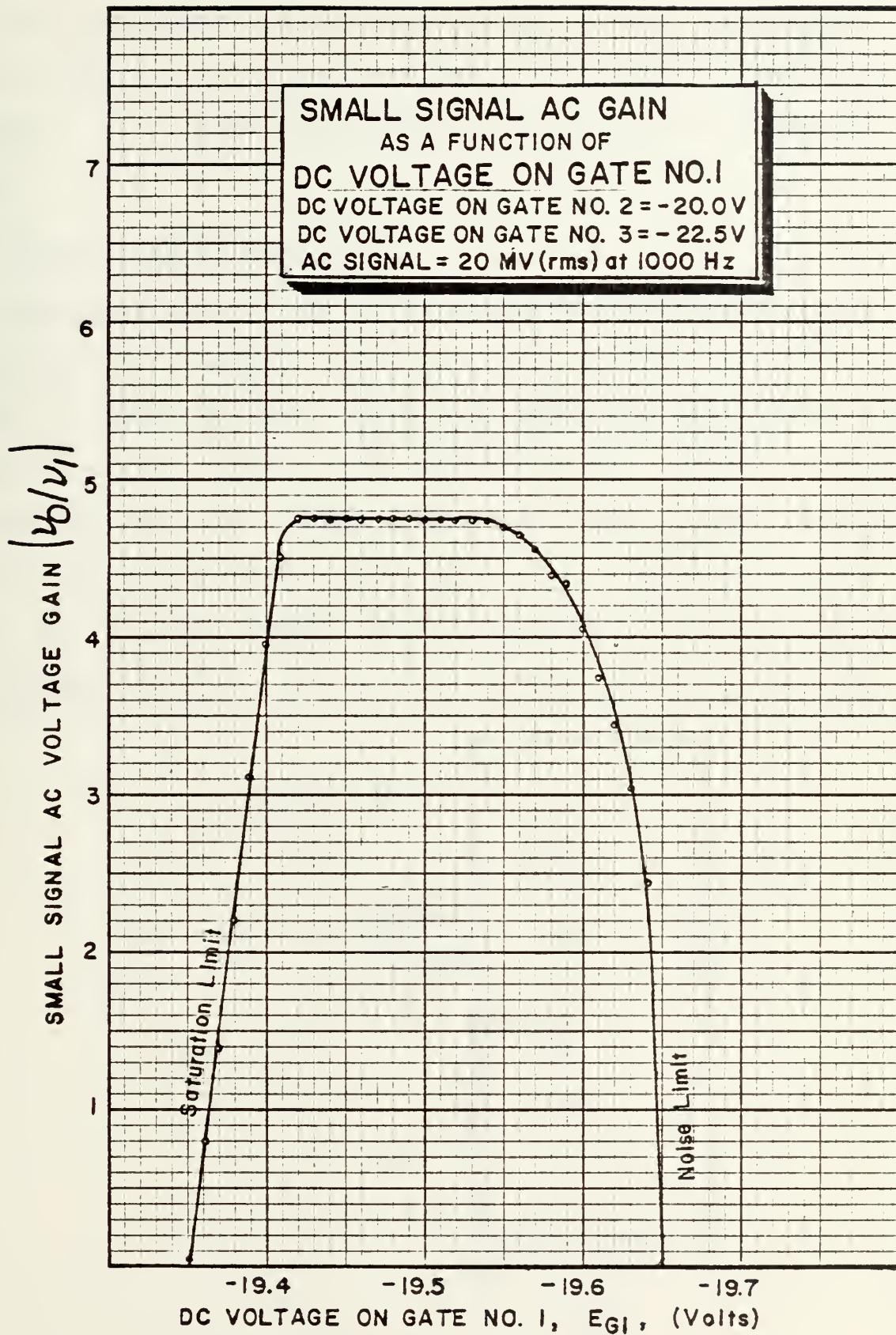


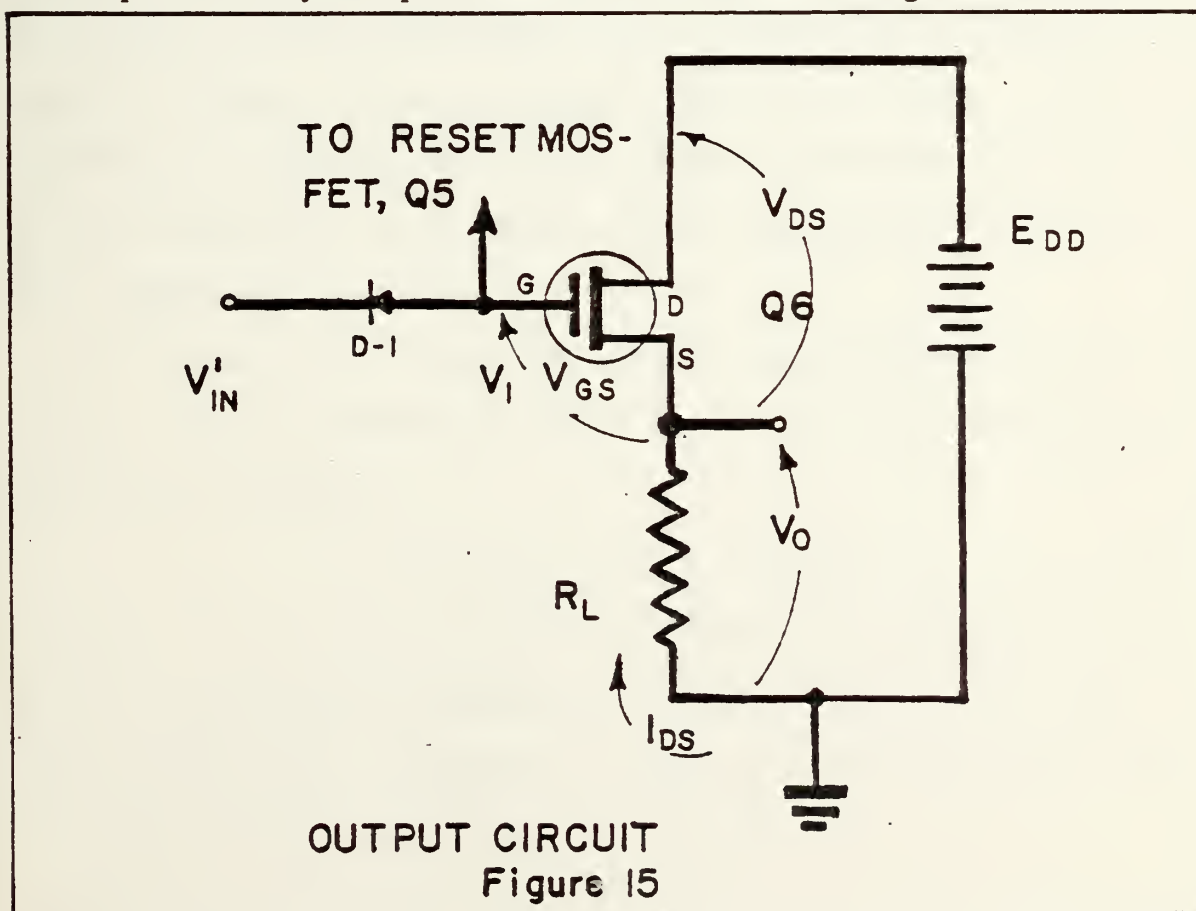
Figure 14



of the curve along the abscissa was noted when the independent parameters of control gate two and three dc-biases were changed. This result was expected based on the DC observations.

#### D. OUTPUT CIRCUIT ANALYSIS

The operation of the output circuit has been previously described in an earlier section of this paper. The circuit, shown in Figure 15, must provide an extremely high impedance input to prevent loading the preceding stage, which in this device was the small charge packet delivered through the channel to the output diode. To achieve this high input impedance, not only was MOSFET circuitry employed, but the circuit was capacitively coupled to the channel through the reverse





biased output diode. While utilization of the transition capacitance of a reverse biased diode does indeed represent a high impedance coupling scheme, it is not without disadvantages. The reverse bias must be maintained. This is an additional requirement on the output circuit. The transition capacitance is nonlinear; i.e., it varies with the applied voltage. It is the purpose of this section of the study to examine these effects on the output voltage as a function of the channel potential immediately adjacent to the output diode within the device.

### 1. Data Curve Fitting

It became apparent that much of the output circuit analysis would require numerical solutions using a computer. The output of such techniques can be presented in tabular or graphical form, but not in closed analytical form. It was desirable to have an ability to reduce such data to an analytical expression that would closely approximate the original numerical solution.

Generally, a curve can be closely approximated by a polynomial. Such a polynomial would have a set of coefficients and be of the form:

$$y = C_1 + C_2x + C_3x^2 + \dots + C_nx^{n-1} \quad (8)$$

At the  $i^{\text{th}}$  data point, where the independent variable is  $x_i$  and the corresponding dependent variable value is  $y_i$ ; the error between the polynomial and the measured data value can be mathematically expressed as follows:



$$e_i = C_1 + C_2 x_i + C_3 x_i^2 + \cdots + C_n x_i^{n-1} - y_i \quad (9)$$

The intent is to evaluate the coefficients in such a manner as to minimize the total of the errors at all data points. It is possible, in fact probable, that individual errors could be either positive or negative. In such an event, building a quantity based on the sum of the errors would produce an invalid conclusion, as large negative errors added to large positive errors could produce a small total. To generate a monotonically increasing function that is an inverse measure of the "goodness" of fit, the sum of the square of the errors is used. That is:

$$M = \sum_{i=1}^m e_i^2 \quad (10)$$

or,

$$M = \sum_{i=1}^m \{ (y_i^2 + C_1^2 + C_2^2 x_i^2 + \cdots + C_n^2 x_i^{2(n-1)}) + \cdots \quad (11)$$

$$\cdots + (2C_1 C_2 x_i + 2C_1 C_3 x_i^2 + \cdots + 2C_1 C_n x_i^{n-1}) + \cdots$$

$$\cdots + (2C_2 C_3 x_i^3 + 2C_2 C_4 x_i^4 + \cdots + 2C_2 C_n x_i^n) + \cdots$$

$$\cdots + (2C_{n-1} C_n x_i^{2n-3}) + \cdots$$

$$\cdots + (-2C_1 y_i - 2C_2 x_i y_i - \cdots - 2C_n x_i^{n-1} y_i) \}$$

To determine the coefficients, it is necessary to determine the partial derivatives of the sum of the square of the errors with respect to each of the  $n$  coefficients. Setting these partial derivatives equal to zero yields a set of  $n$  simultaneous linear equations. The solution vector of this set of equations is the set of  $n$  coefficients what provides a polynomial of degree  $n-1$  that best fits the data points.



That is, the coefficients have been so selected as to minimize the summation of the square of errors at each data point. This set of equations is made up of several summation terms formed from the data points. In the makeup of the equations, wherever the summation symbol appears, it indicates the summation of the variable term following it for all data points from 1 to m, the total number of data points. The set of equations to be solved is then:

$$\begin{array}{rcl}
 C_1^m & + C_2 \sum x_i + C_3 \sum x_i^2 + \dots + C_n \sum x_i^{n-1} & = \sum y_i \\
 C_1 \sum x_i & + C_2 \sum x_i^2 + \dots + C_n \sum x_i^n & = \sum y_i x_i \\
 C_1 \sum x_i^2 & + \dots & = \sum y_i x_i^2 \\
 \vdots & & \vdots \\
 C_1 \sum x_i^{n-1} & + C_2 \sum x_i^n + \dots + C_n \sum x_i^{2(n-1)} & = \sum y_i x_i^{n-1}
 \end{array} \tag{12}$$

To facilitate the output circuit analysis, a computer program was written to generate the above set of equations and solve for the coefficients for any value of n from 2 to 10, with m data points. For additional utility, the program included the capability to fit data to a power function:

$$y = ax^b \tag{13}$$

and the exponential function:

$$y = ae^{bx} \tag{14}$$

Both of these functions can be manipulated for best data fit with the same polynomial approach, with the following modifications:

1. Use n = 2, that is the best fit straight line,



2. For the power function, supply the natural logarithm of  $x$ , rather than  $x$ , as the data,
3. Supply the natural logarithm of  $y$  as data,
4. Evaluate the constant  $a$ , as the  $\exp(C_1)$  in both cases, and
5. When printing out the data, convert back to the original data by using  $\exp(y_i)$  and in the case of the power function,  $\exp(x_i)$ .

The computer program that was developed is appended hereto as Appendix D. In addition to the form of the curve, the program will supply, as part of the output, the calculated values of the dependent variable, the data points, and the sum of the square of the errors. In a case where no information is available as to the type of curve the data represents, the program is run to try the power function, the exponential function, and all polynomials to degree 9. The sum of the square of the errors will be smallest for the best fit curve.

## 2. Output MOSFET Characteristics

To analyze the output of the circuit in Figure 15, a knowledge of the characteristics of the output MOSFET is required. As previously discussed in section IV.F., the manufacturer provided data on the gate to source voltage and the drain to source current of four sample devices. This data is presented in Table I.

The data for device number 3, was rejected as being non-typical of the devices studied. The remaining data was processed using the data fit routine described in the preceding section. The data was processed as:



$$y_i = \sqrt{I_{DS_i}} \quad (15)$$

$$x_i = V_{DS_i} = V_{GS_i} \quad (16)$$

$$n = 2 \quad (17)$$

The results of the program are tabulated in Appendix A hereto and are displayed graphically in Figure 10. The average error in the fit was  $1.29 \times 10^{-10}$  amps. The equation describing the current-voltage relationship is:

$$I_{DS} = -k(V_{GS} - V_T)^2 \quad (18)$$

where:  $k = 2.2032 \times 10^{-6} \text{ amp/volt}^2 \quad (19)$

$$V_T = -1.76466 \text{ volts} \quad (20)$$

Recalling that the length of the channel in the direction of current flow is smaller than the designed or masked length,  $L$ , because of the  $p^+$ -diffusions proceeding laterally under the mask by a distance called the junction depth,  $x_j$ . Then:

$$\ell = L - 2x_j \quad (21)$$

In the case of the experimental device:

$$W = 0.4 \text{ mils} \quad (22)$$

$$L = 0.6 \text{ mils} \quad (23)$$

$$x_j = 0.06 \text{ mils} \quad (24)$$

$$\ell = 0.48 \text{ mils} \quad (25)$$

With this geometry, the conduction factor,  $k'$ , is:

$$k' = \frac{\mu_p \epsilon_r \epsilon_0}{2t_{ox}} = \frac{\ell k}{W} = 2.2644 \times 10^{-6} \text{ amps/volt}^2 \quad (26)$$

Using the parameters obtained, it was possible to cons-



Table I

Drain to Source Current - $I_{DS}$ ( $\mu A$ )	Drain to Source Voltage - $V_{DS} = V_{GS}$ (volts) <sup>DS</sup>			
	Device 1	Device 2	Device 3	Device 4
0.1	2.04	2.04	1.84	1.96
1.0	2.50	2.50	2.30	2.44
4.0	3.14	3.14	2.91	3.08
9.0	3.76	3.77	3.52	3.75
16.0	4.42	4.41	4.15	4.37
25.0	5.08	5.10	4.79	5.07
36.0	5.80	5.80	5.47	5.07
49.0	6.46	6.46	4.57	6.50
64.0	7.15	7.16	6.82	7.20
81.0	7.85	7.87	7.49	7.91

tract the drain characteristics of the output MOSFET. The basic Sah model [Ref. 7] of the transistor, assuming no source to drain resistance, indicates that the drain to source current will be a constant for all values of the drain to source voltage once the transistor is in saturation. This model also provided expressions for the current under conditions of saturation, equation (4), and non-saturation, equation (5). The saturation relationship has already been used to define the threshold voltage and the gain parameter. Using these values, the two voltage-current relationships were used to establish the drain characteristic curves shown in Figure 16. A load line for operation into a 50,000 ohm load resistance is also plotted on the curves. This value or load resistance was typical of the conditions used during the experimental portion of this study.

### 3. Output Diode Effects

Capacitively coupling the output MOSFET to the CCD channel through a reverse biased diode provides the required



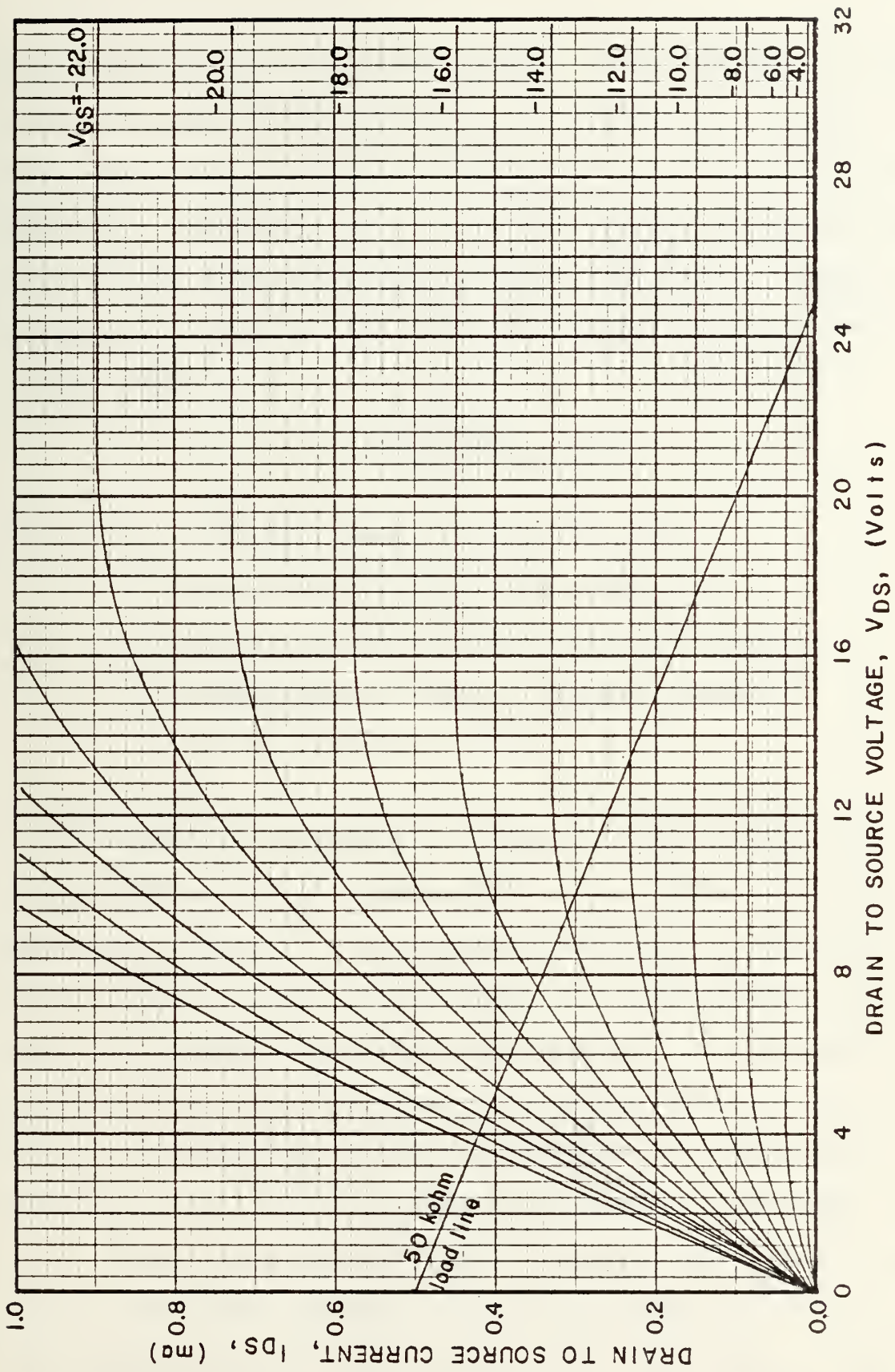


Figure 16

Typical output MOSFET drain characteristics.



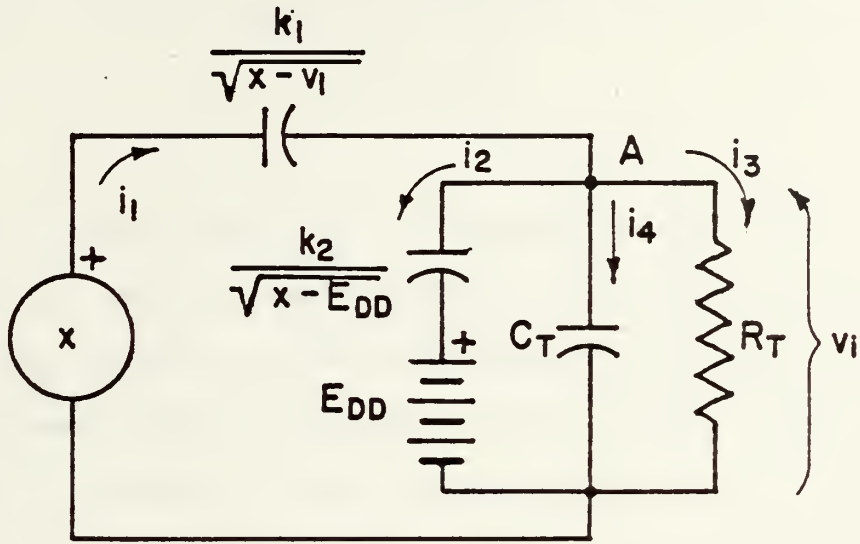
high impedance load for the channel. Unfortunately, it presents the complication of having the capacitance of the coupling capacitor, the diode, vary as a function of the voltage across it. Assuming that the reverse biased junctions involved with the output circuit are made with abrupt changes from n-region to p-region, the value of the junction capacitance is [Ref. 8]:

$$C = \sqrt{\frac{q_0 \epsilon_r \epsilon_0 N_d}{2V_a}} \text{ farad/cm}^2 \quad (27)$$

where:  $q_0$  = electronic charge,  $1.602 \times 10^{-19}$  coulomb  
 $\epsilon_r$  = relative permittivity of the oxide, 11.8  
 $\epsilon_0$  = permittivity of free space,  $8.854 \times 10^{-14}$  farad/cm  
 $N_d$  = concentration of donors in n-region, atoms/cm<sup>3</sup>  
 $V_a$  = applied potential in volts.

To assist in analyzing the effect of the output diode, the simplified circuit representation in Figure 17 was used. The input potential, that potential adjacent to the cathode of the output diode, is the signal,  $x$ . The current  $i_1$ , flows through the output diode and then branches into currents  $i_2$ ,  $i_3$  and  $i_4$ . Current  $i_2$ , flows through the reverse biased p-n junction represented by the reset MOSFET, Q5. Current  $i_3$ , represents the leakage through the substrate, the input resistance of the output MOSFET and the pinched off channel resistance of the reset MOSFET. Current  $i_4$ , represents the current into the gate of the output MOSFET, Q6. The signal output is  $V_i$ , the input voltage to the output MOSFET. Writing the nodal





EQUIVALENT CIRCUIT SEEN BY THE OUTPUT DIODE  
Figure 17

equations for node A:

$$i_1 = i_2 + i_3 + i_4 \quad (28)$$

Now, in general:

$$i = \frac{d}{dt}(CV) \quad (29)$$

Then, for the circuit in Figure 17:

$$\frac{k_1}{2\sqrt{x-V_i}} \frac{dx}{dt} - \frac{k_1}{2\sqrt{x-V_i}} \frac{dV_i}{dt} = \frac{k_2}{2\sqrt{V_i-E_{DD}}} \frac{dV_i}{dt} + \frac{V_i}{R_T} + C_T \frac{dV_i}{dt} \quad (30)$$

or, solving for the derivative of the output with respect to time:

$$\frac{dV_i}{dt} = \frac{\frac{k_1}{2\sqrt{x-V_i}} \frac{dx}{dt} - \frac{1}{R_T} V_i}{\frac{k_1}{2\sqrt{x-V_i}} + C_T + \frac{k_2}{2\sqrt{V_i-E_{DD}}}} \quad (31)$$

where:

$$k_1 = A_1 \sqrt{\frac{q_0 \epsilon_r \epsilon_0 N_d}{2}} \quad (32)$$



$$k_2 = A_2 \sqrt{\frac{q_0 \epsilon_r \epsilon_0 N_d}{2}} \quad (33)$$

$$C_T = \frac{\epsilon_r \epsilon_0 A_3}{d} \quad (34)$$

Some of these quantities are known, but for others assumptions must be made. Every assumption presents a possible error in the analysis of the experimental circuit, but the values assumed will be typical of those seen in semiconductor technology. Further, if the assumptions depart from the experimental device, they will still provide meaningful analysis of the type of output circuit employed.

The value of the oxide thickness,  $d$  in equation (34) is known as 1000Å. Likewise, the values of  $q_0$ ,  $N_d$ ,  $E_{DD}$ ,  $\epsilon_r$  and  $\epsilon_0$  are established quantities. The initial conditions, the input voltage function,  $x$ , and the areas  $A_1$ ,  $A_2$  and  $A_3$ , are not so well defined.

The area of the output diode,  $A_1$ , is taken to be a rectangle 2.0 mils long by 0.25 mils wide. The area of the reset MOSFET source diffusion is taken to be 0.4 mils long by 0.25 mils wide. The output MOSFET gate is 0.4 mils by 0.6 mils. The distributed resistance,  $R_T$ , is assumed to be  $5 \times 10^9$  ohms.

Since the quiescent output voltage was experimentally seen to be about -12 volts, it can be seen from Figure 16, that the quiescent gate voltage must be about -24 volts. The initial value of the variable,  $V_i$ , is then taken to be -24.0 volts.

The input function is taken to be a voltage step from -25 volts to -12 volts at time equal 15  $\mu$ sec returning to -25 volts at the time, 47  $\mu$ sec.



Using the known values and the assumed quantities, the numerical constants now become:

$$k_1 = 2.2951 \times 10^{-14} \text{ farad-volt}^{\frac{1}{2}} \quad (35)$$

$$k_2 = 5.902 \times 10^{-15} \text{ farad-volt}^{\frac{1}{2}} \quad (36)$$

$$C_T = 1.618 \times 10^{-13} \text{ farad} \quad (37)$$

A computer program to solve the general initial value problem:

$$\frac{dy}{dt} = f(x, y, z) \quad (38)$$

$$\text{where:} \quad x = g(t) \quad (39)$$

$$z = \frac{dx}{dt} \quad (40)$$

$$\text{and:} \quad y = y_0 \quad (41)$$

$$\text{when:} \quad t = 0 \quad (42)$$

was developed using fourth order Runge-Kutta methods. This program is listed in Appendix B hereto. The program was executed and the results are tabulated in Appendix A and graphically displayed in Figure 18.

The results of the solution to the differential equation represent the response of the output diode to an input pulse in the CCD channel. This response would represent one sample of the output signal. In order to determine the linearity of the output diode to an input waveform, of which the function  $g(t)$  is only one sample; and which will be processed by a sample and hold circuit, it was necessary to modify the



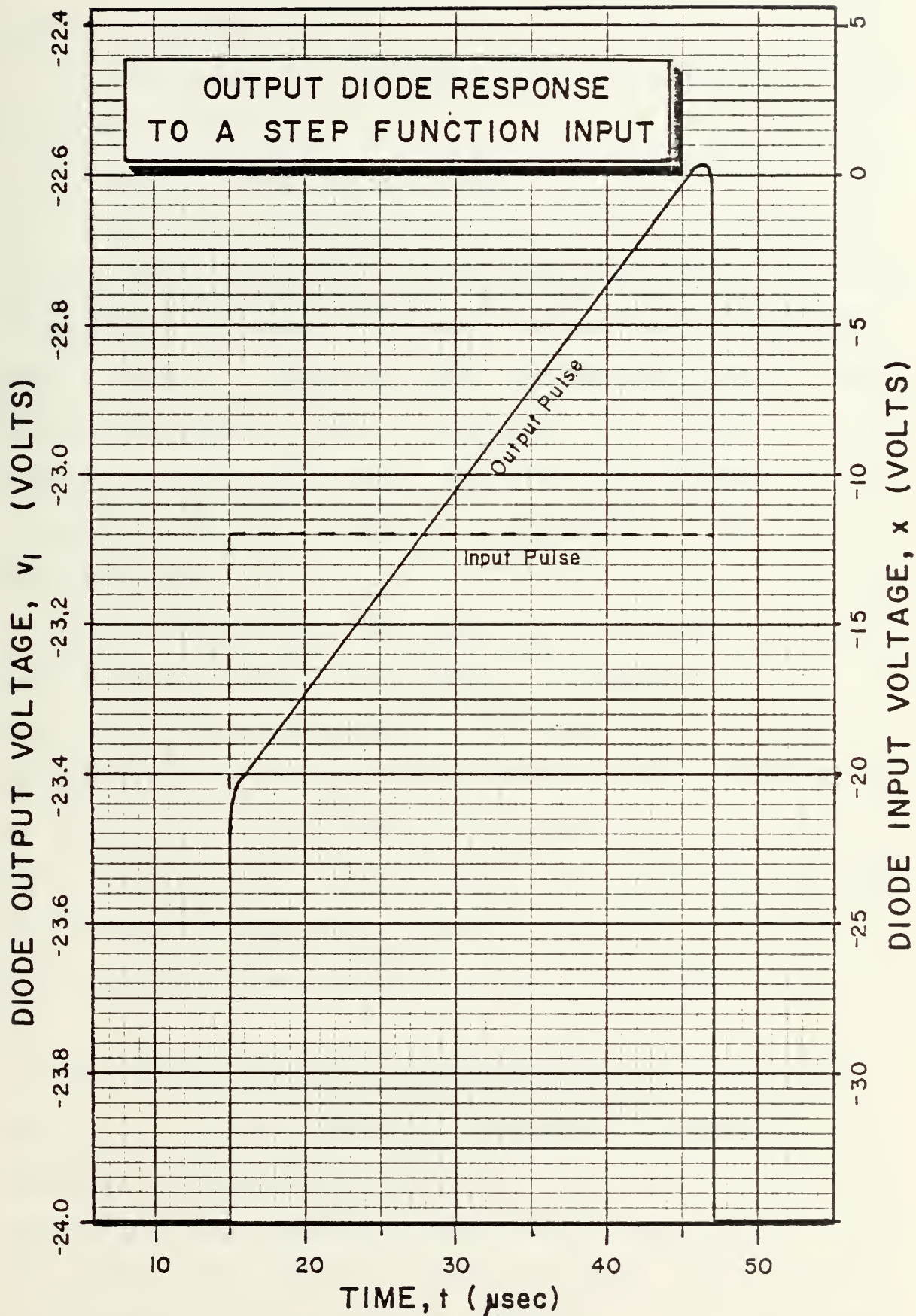


Figure 18



computer program.

This was done, and the results are discussed as the input to the source follower.

#### 4. Input to the Source Follower

While the transient analysis of the output diode to a step function provides the waveform of the input to the output MOSFET, it does not represent the response to the signal input. Rather, it represents the response to a single sampling of the signal. What is required is the relationship between the peak amplitude of the potential adjacent to the output diode in the CCD channel and the peak of the output diode response.

To accomplish this, the differential equation solution routine was modified. The program was modified to solve equation (31) forty-one times. The amplitude of the channel potential step function was increased from -20 volts to -10 volts in 0.25 volt steps. The duration of the step and the quiescent value of the voltages were maintained as before. The program was required to provide an output of only the peak input pulse amplitude,  $x$ , and the peak output pulse,  $V_i$ .

The modified program is appended hereto in Appendix C. The results of the program are tabulated in Appendix A and presented graphically in Figure 19. The solution data from this program was used as an input to the curve fitting routine. It was found that the best fit of the results was with a polynomial of degree 3. The expression for the peak MOSFET



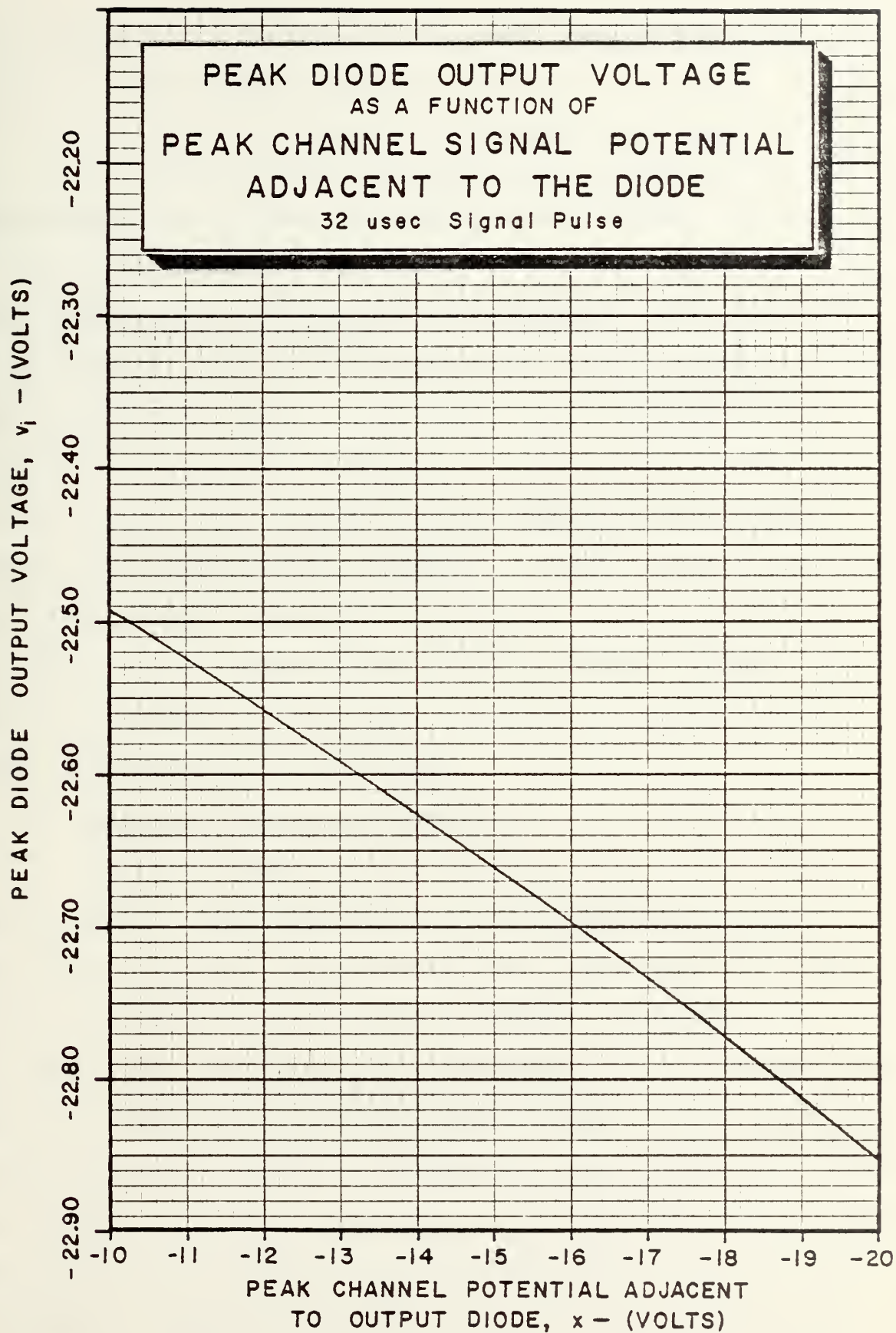


Figure 19



input voltage as a function of the peak channel potential adjacent to the output diode is:

$$-V_i = 22.15 + 3.81 \times 10^{-2} |x| - 6.15 \times 10^{-4} |x|^2 + 2.33 \times 10^{-5} |x|^3 \quad (46)$$

The average error of fit was found to be  $2.41 \times 10^{-5}$  volts.

An advantage of presenting the results as a polynomial is that a measurement of linearity is available. The value of the coefficient of  $x$  to the first power may be ratioed to the sum of the coefficients of all powers of  $x$ , to express the fraction of linearity. Likewise, the sum of the coefficients of all  $x$  terms with exponents larger than one is an expression of the departure from linearity. Using the more precise coefficient values tabulated in Appendix A, it is seen that the output of the output diode is 98.35 percent linear. Or, only 1.65 percent of the output variation is caused by non-linear relationships to the input.

## 5. Output of the Source Follower

The next element in the output circuit is the output MOSFET itself. Using the model of the transistor that has been used throughout, an expression for the output as a function of the MOSFET input can be developed. Referring to Figure 20 for nomenclature, the expression for the output current as a function of the gate input voltage will be developed. By examination of Figure 16 remembering that the output quiescent voltage was about -12 volts, it is seen that with a drain bias supply of -25 volts, that the transistor is always in saturation. Utilizing equation (18), the output current is seen to be:



$$I_{DS} = -k(V_i - V_o - V_T)^2 \quad (47)$$

$$\text{but,} \quad V_o = I_{DS} R \quad (48)$$

$$\text{then,} \quad V_o = -kR(V_i - V_o - V_T)^2, \quad (49)$$

and by simple manipulation,

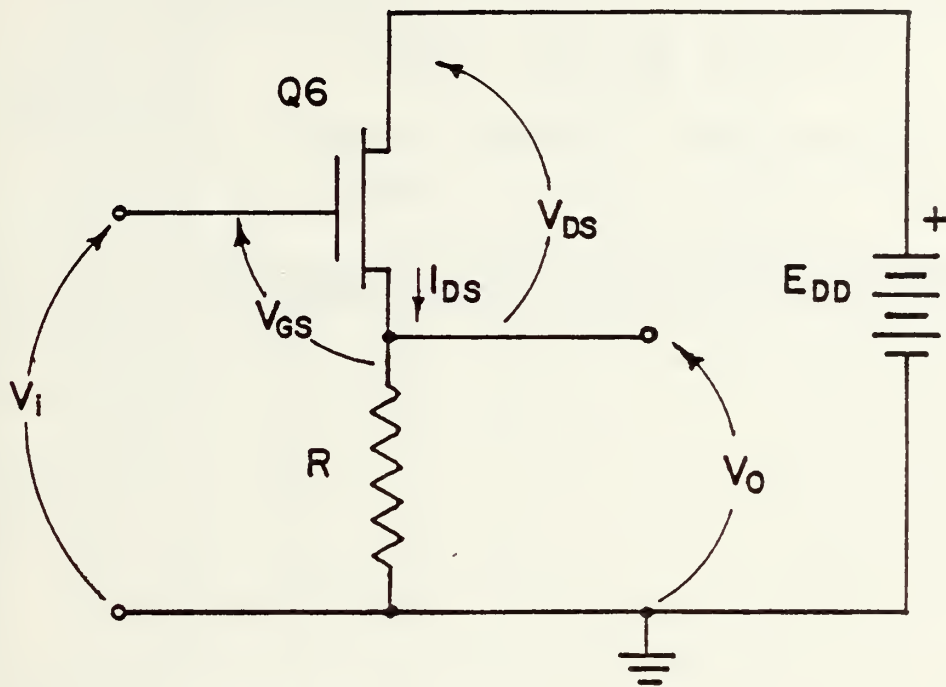
$$V_o = -\frac{1}{2}\{2(V_T - V_i) + \frac{1}{kR}\} \pm \frac{1}{2}\sqrt{\{2(V_T - V_i) + \frac{1}{kR}\}^2 - 4(V_i^2 + V_T^2 - 2V_i V_T)} \quad (50)$$

This output relationship was evaluated using the computer with the program listed in Appendix E. The input voltage,  $V_i$ , was programed into the calculation as the third degree polynomial developed in the preceding section. The negative option for the radical in equation (50) was ignored in the evaluation, since it would produce output voltages more negative than the drain bias voltage,  $E_{DD}$ , a physical impossibility.

The results of the computer run, then, was a tabulated listing of the output voltage at the source follower load resistor as a function of the channel potential adjacent to the output diode within the CCD. This is the relationship that was desired as a result of the output circuit analysis. The results are tabulated in Appendix A, and presented graphically in Figure 21. Visually, the output voltage dependence on the channel peak potential appears quite close to a linear relationship.

Once again, the curve fitting program was employed to





SIMPLIFIED OUTPUT CIRCUIT

Figure 20

determine an analytical expression for the output voltage pulse peak as a function of the peak potential in the CCD channel adjacent to the output diode. The best fit was found with a polynomial of degree 3. The functional relationship is:

$$-V_o = 10.58 + 2.72 \times 10^{-2} |x| - 4.98 \times 10^{-4} |x|^2 + 1.78 \times 10^{-5} |x|^3 \quad (51)$$

The average error was found to be  $6.77 \times 10^{-6}$  volts.

Once again using the more precise coefficients in Appendix A, the output circuit is 98.14 percent linear. That is, only 1.86 percent of the variation in the peak output voltage due to the channel potential pulse peak is contributed by higher order, or nonlinear, terms.



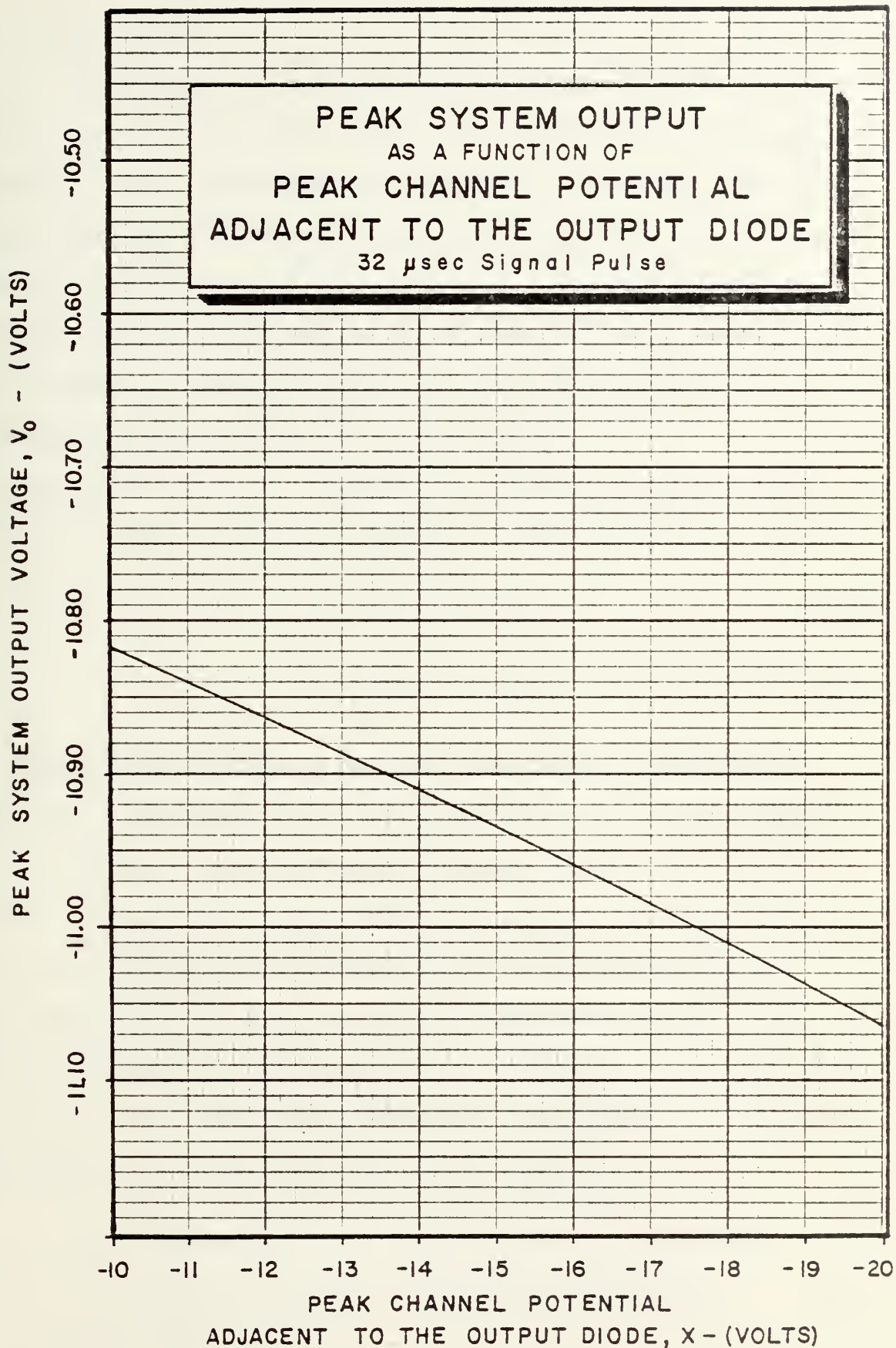


Figure 21



## E. LINEAR MODEL

If electronic devices can be operated so that the non-linear distortion is small, then they can often be approximated by linear equations and circuits. In such cases, all the procedures of linear-circuit analysis can be applied and complex circuits can be analyzed with a minimum of effort. In this section, a linear model of the CCD in an analog signal processing mode is suggested, but no experimentally determined parameter values are provided.

The currents of the network in Figure 22 can be represented as linear functions of the voltages. Thus,

$$I_1 = y_{11}V_1 + y_{12}V_2 \quad (52)$$

$$I_2 = y_{21}V_1 + y_{22}V_2 \quad (53)$$

The parameters of these equations are termed  $y$  parameters. They have the dimensions of admittances. It is most convenient to measure these parameters under short-circuit conditions. It was the experimental application of this concept that proved beyond the capabilities of this experimenter. The intent, was to apply a voltage generator to the input gate and short-circuit the output, or vice versa. Or, failing that, with the circuit otherwise operating, to determine the parameters from the definitions, that is:

$$y_{11} = \frac{\partial I_1}{\partial V_1}, \text{ Short-circuit input driving point admittance} \quad (54)$$

$$y_{21} = \frac{\partial I_2}{\partial V_1}, \text{ Short-circuit forward transfer admittance} \quad (55)$$



$$y_{12} = \frac{\partial I_1}{\partial V_2}, \text{ Short-circuit reverse transfer admittance} \quad (56)$$

$$y_{22} = \frac{\partial I_2}{\partial V_2}, \text{ Short-circuit output driving point admittance} \quad (57)$$

In working with the CCD, it became apparent that little or no short-circuit reverse transfer admittance existed. In light of the manner in which the CCD is fabricated and functions, this is not unreasonable. It was also apparent that the short-circuit input driving point admittance was small and mainly capacitive. The arrangement of the output circuit would indicate that the short-circuit output driving point admittance would be the reciprocal of the output MOSFET's dynamic drain-source resistance. The quantity that would be peculiar to a CCD was the short-circuit forward transfer admittance,  $y_{21}$ . This quantity would have to indicate the sampled nature of the output, as well as the time delay of the output with respect to the input. Neglecting the output dynamic drain-source resistance, such a quantity would be:

$$y_{21} = \frac{dI_o}{dV_i} \left( u\left(t - \frac{nN}{f_c}\right) - u\left(t - \frac{nN}{f_c} - \tau\right) \right) \quad (58)$$

where:

$\frac{dI_o}{dV_i}$  = The slope of the dc gain curve.

$u(t)$  = The unit step function

$n$  = The sequence of consecutive integers that best represents the sampling during the period of interest.

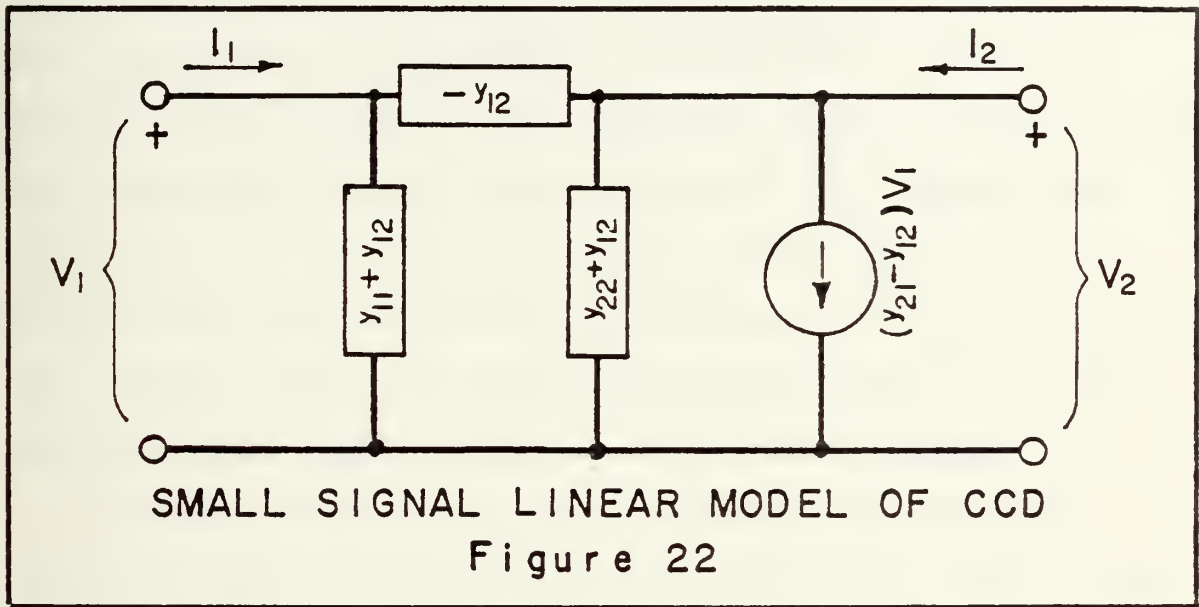
$N$  = The number of charge-coupled structures

$f_c$  = The phase clocking frequency

$\tau$  = The duration of the sampling pulse.



In arriving at N, the number of charge-coupled structures, a structure constitutes one delay element, that is, in a two-phase device, a set of four consecutive gates connected to the two different phase clocking signals.



In those applications where multiple inputs are used, a modification would have to be imposed on the model. Each input would have its own input driving point admittance; but beyond that point, each input would have to be ratioed based on its effect on the output current. The ratioed potentials would act on a summing point, the voltage of which would be the input voltage to the expression for the model's dependent current source.



## VI. CONCLUSIONS

It was established that the two-phase charge-coupled shift register could be used to process analog signals. In the course of such processing, a consistent gain was displayed and an electronically controlled delay could be inserted. The output of the charge-coupled shift register was a sampled version of the input signal, but a sample and hold circuit restored the wholly analog nature to the output signal. Little nonlinear distortion was observed over a small range of input signal level, i.e., 0.1 to 0.2 volts.

Further, it was found that the charge-coupled shift register could be made to function as an analog signal adder-subtractor with good linearity. Once again the dynamic range over which linearity could be achieved was 0.1 to 0.2 volts. The small dynamic range is attributed to the small surface potential wells of the experimental device. If more charge could be transferred, a larger dynamic range would be evidenced.

An analysis of the output circuit employed established that very slight nonlinearities were introduced by the output technique used on the experimental device.

Finally, a linear model of the charge-coupled shift register is proposed.



# TABULATION OF COMPUTER OUTPUTS SATURATION CHARACTERISTICS OF OUTPUT MOSFET.

POLYNOMIAL CURVE FIT:

$$Y = (-2.61432E-3) + (1.45432E-3) * X + (0) * X^2 + \dots \\ + (0) * X^3 + (0) * X^4 + \dots \\ + (0) * X^5 + (0) * X^6 + \dots \\ + (0) * X^7 + (0) * X^8 + \dots \\ + (0) * X^9$$

THE VALUE OF THE GAIN PARAMETER,  $K$ , IS:  $2.27322E-6$

THE VALUE OF THE THRESHOLD VOLTAGE IS:  $-1.76466$

DATA POINTS AND CALCULATED VALUES OF Y

VALUE OF X	VALUE OF Y	CALCULATED Y
-2.44	-3.16224E-4	-4.48686E-4
-2.44	-3.16224E-4	-4.48686E-4
-1.96	-3.16228E-4	-2.24444E-4
-2.5	-4.441	-1.49147E-3
-2.5	-4.441	-1.49147E-3
-2.44	-4.441	-1.44241E-3
-3.14	-4.442	-2.44143E-3
-3.14	-4.442	-2.44143E-3
-3.44	-4.442	-1.35235E-3
-3.76	-4.443	-2.36171E-3
-3.77	-4.443	-2.37655E-3
-3.75	-4.443	-2.34657E-3
-4.42	-4.444	-3.44136E-3
-4.41	-4.444	-3.92652E-3
-4.37	-4.444	-3.86714E-3
-5.44	-4.445	-4.42161E-3
-5.1	-4.445	-4.95459E-3
-5.47	-4.445	-4.94617E-3
-5.4	-4.446	-5.48972E-3
-5.4	-4.446	-5.48972E-3
-5.4	-4.446	-5.48972E-3
-6.46	-4.447	-6.96937E-3
-6.46	-4.447	-6.96937E-3
-6.5	-4.447	-7.42674E-3
-7.15	-4.448	-7.99354E-3
-7.16	-4.448	-8.44839E-3
-7.2	-4.448	-8.46776E-3
-7.45	-4.449	-9.43257E-3
-7.47	-4.449	-9.76225E-3
-7.91	-4.449	-9.12163E-3

THE SUM OF THE SQUARE OF THE ERRORS =  $1.16485E-7$



ODD OUTPUT DIODE RESPONSE TO A STEP FUNCTION INPUT

VALUE OF T	VALUE OF X	VALUE OF Y
1.4445E-5	-25	-24
1.44452E-5	-25	-23.8215
1.59954E-5	-12	-23.4446
1.69954E-5	-12	-23.3768
1.79454E-5	-12	-23.3491
1.83354E-5	-12	-23.3214
1.99949E-5	-12	-23.2937
2.29949E-5	-12	-23.2661
2.19949E-5	-12	-23.2384
2.29949E-5	-12	-23.2143
2.39944E-5	-12	-23.1833
2.49949E-5	-12	-23.1558
2.59949E-5	-12	-23.1283
2.69949E-5	-12	-23.1008
2.79449E-5	-12	-23.0734
2.83449E-5	-12	-23.046
2.99445E-5	-12	-23.0187
3.29948E-5	-12	-22.9913
3.19944E-5	-12	-22.964
3.29948E-5	-12	-22.9366
3.39944E-5	-12	-22.9095
3.49948E-5	-12	-22.8823
3.59948E-5	-12	-22.8551
3.69948E-5	-12	-22.828
3.7944E-5	-12	-22.8009
3.89947E-5	-12	-22.7735
3.94447E-5	-12	-22.7467
4.09947E-5	-12	-22.7197
4.19947E-5	-12	-22.6927
4.29947E-5	-12	-22.6653
4.39947E-5	-12	-22.6386
4.49947E-5	-12	-22.612
4.59947E-5	-12	-22.5851
4.69947E-5	-12	-22.5581
4.79497E-5	-25	-23.181

TIME: 47.44 SECS.

READY



PEAK OUTPUT DIODE VOLTAGE AS A FUNCTION OF  
PEAK CHANNEL VOLTAGE

X PEAK	Y PEAK
-10	-22.4928
-10.25	-22.501
-10.5	-22.5091
-10.75	-22.5173
-11	-22.5256
-11.25	-22.5338
-11.5	-22.5421
-11.75	-22.5504
-12	-22.5588
-12.25	-22.5672
-12.5	-22.5756
-12.75	-22.584
-13	-22.5925
-13.25	-22.601
-13.5	-22.6096
-13.75	-22.6182
-14	-22.6268
-14.25	-22.6355
-14.5	-22.6443
-14.75	-22.653
-15	-22.6618
-15.25	-22.6707
-15.5	-22.6796
-15.75	-22.6886
-16	-22.6976
-16.25	-22.7067
-16.5	-22.7158
-16.75	-22.725
-17	-22.7343
-17.25	-22.7436
-17.5	-22.753
-17.75	-22.7625
-18	-22.7721
-18.25	-22.7818
-18.5	-22.7916
-18.75	-22.8015
-19	-22.8115
-19.25	-22.8216
-19.5	-22.8319
-19.75	-22.8423
-20	-22.8529

TIME: 1961.21 SECS.



# PEAK DIODE OUTPUT VOLTAGE

As a Function of

PEAK CHANNEL SIGNAL POTENTIAL ADJACENT TO THE DIODE

(Least Squares Curve Fit)

RUN

51DL02

00:44

04-DEC-75

OUTPUT VOLTAGE AS A FUNCTION OF INPUT VOLTAGE

POLYNOMIAL CURVE FIT:

$$Y = (22.15) + (3.89940E-2) * X + (-6.15105E-4) * X^2 + \dots \\ + (2.33133E-5) * X^3 + (0) * X^4 + \dots \\ + (0) * X^5 + (0) * X^6 + \dots \\ + (0) * X^7 + (0) * X^8 + \dots \\ + (0) * X^9$$

DATA POINTS AND CALCULATED VALUES OF Y

VALUE OF X	VALUE OF Y	CALCULATED Y
10	22.4925	22.4927
10.25	22.501	22.5009
10.5	22.5091	22.5092
10.75	22.5173	22.5174
11	22.5256	22.5256
11.25	22.5338	22.5339
11.5	22.5421	22.5422
11.75	22.5504	22.5505
12	22.5588	22.5588
12.25	22.5672	22.5672
12.5	22.5756	22.5756
12.75	22.584	22.584
13	22.5925	22.5925
13.25	22.601	22.601



Value of X	Value of Y	Calculated Y
13.5	22.6095	22.6095
13.75	22.6182	22.6181
14	22.6263	22.6267
14.25	22.6355	22.6354
14.5	22.6443	22.6441
14.75	22.653	22.6529
15	22.6618	22.6617
15.25	22.6707	22.6706
15.5	22.6795	22.6795
15.75	22.6886	22.6885
16	22.6976	22.6975
16.25	22.7067	22.7066
16.5	22.7158	22.7158
16.75	22.725	22.7251
17	22.7343	22.7344
17.25	22.7436	22.7435
17.5	22.753	22.7532
17.75	22.7625	22.7627
18	22.7721	22.7724
18.25	22.7818	22.7821
18.5	22.7916	22.7918
18.75	22.8015	22.8017
19	22.8115	22.8116
19.25	22.8216	22.8217
19.5	22.8319	22.8319
19.75	22.8423	22.842
20	22.8529	22.8523

THE SUM OF THE SQUARE OF THE ERRORS = 9.74491E-7

TIME: 2.92 SECS.

READY



OUTPUT OF SOURCE FOLLOWER AS A FUNCTION OF  
CHANNEL VOLTAGE IN CCD

CHANNEL VOLTAGE	OUTPUT VOLTAGE	IN SATURATION
-10	-10.8182	YES
-10.25	-10.8239	YES
-10.5	-10.8295	YES
-10.75	-10.8352	YES
-11	-10.8408	YES
-11.25	-10.8465	YES
-11.5	-10.8522	YES
-11.75	-10.8579	YES
-12	-10.8636	YES
-12.25	-10.8693	YES
-12.5	-10.8751	YES
-12.75	-10.8809	YES
-13	-10.8867	YES
-13.25	-10.8925	YES
-13.5	-10.8984	YES
-13.75	-10.9043	YES
-14	-10.9102	YES
-14.25	-10.9162	YES
-14.5	-10.9221	YES
-14.75	-10.9282	YES
-15	-10.9342	YES
-15.25	-10.9403	YES
-15.5	-10.9465	YES
-15.75	-10.9526	YES
-16	-10.9588	YES
-16.25	-10.9651	YES
-16.5	-10.9714	YES
-16.75	-10.9778	YES
-17	-10.9842	YES
-17.25	-10.9906	YES
-17.5	-10.9971	YES
-17.75	-11.0037	YES
-18	-11.0103	YES
-18.25	-11.017	YES
-18.5	-11.0237	YES
-18.75	-11.0305	YES
-19	-11.0373	YES
-19.25	-11.0442	YES
-19.5	-11.0512	YES
-19.75	-11.0582	YES
-20	-11.0653	YES

TIME: 1.02 SECS.



# PEAK SYSTEM OUTPUT VOLTAGE

As a Function of

PEAK CHANNEL POTENTIAL ADJACENT TO THE OUTPUT DIODE

RUN (Least Squares Curve Fit)

B10L02 AM:11 05-DEC-75

OUTPUT VOLTAGE FROM MOSFET SOURCE FOLLOWER  
AS A FUNCTION OF CHANNEL VOLTAGE.

POLYNOMIAL CURVE FIT:

$$Y = ( 10.576 ) + ( 2.72134E-2 ) * X + ( -4.97656E-4 ) * X^2 + \dots \\ + ( 1.77696E-5 ) * X^3 + ( 0 ) * X^4 + \dots \\ + ( 0 ) * X^5 + ( 0 ) * X^6 + \dots \\ + ( 0 ) * X^7 + ( 0 ) * X^8 + \dots \\ + ( 0 ) * X^9$$

DATA POINTS AND CALCULATED VALUES OF Y

VALUE OF X	VALUE OF Y	CALCULATED Y
10	10.8182	10.8182
10.25	10.8239	10.8238
10.5	10.8295	10.8295
10.75	10.8352	10.8351
11	10.8408	10.8408
11.25	10.8465	10.8465
11.5	10.8522	10.8522
11.75	10.8579	10.8579
12	10.8636	10.8636
12.25	10.8693	10.8694
12.5	10.8751	10.8751
12.75	10.8809	10.8809
13	10.8867	10.8867
13.25	10.8925	10.8926



Value of X	Value of Y	Calculated Y
13.5	10.8984	10.8984
13.75	10.9043	10.9043
14	10.9102	10.9102
14.25	10.9162	10.9162
14.5	10.9221	10.9222
14.75	10.9282	10.9282
15	10.9342	10.9342
15.25	10.9403	10.9403
15.5	10.9465	10.9464
15.75	10.9526	10.9526
16	10.9588	10.9588
16.25	10.9651	10.9651
16.5	10.9714	10.9714
16.75	10.9778	10.9777
17	10.9842	10.9841
17.25	10.9906	10.9906
17.5	10.9971	10.9971
17.75	11.0037	11.0036
18	11.0103	11.0103
18.25	11.017	11.0169
18.5	11.0237	11.0237
18.75	11.0305	11.0305
19	11.0373	11.0373
19.25	11.0442	11.0442
19.5	11.0512	11.0512
19.75	11.0582	11.0583
20	11.0653	11.0654

THE SUM OF THE SQUARE OF THE ERRORS = 7.70513E-8

TIME: 2.88 SECS.

READY



```

100' NAME--BIDLA1
110'
120' DESCRIPTION--SOLVES THE INITIAL VALUE PROBLEM,
130'
140'     Y'=F(X,Y,Z)
150'     WHERE:  X=G(T)
160'             Y(T0)=Y0
170'             Z(T)=X'
180'
190' SOURCE--RUNGE-KUTTA (FOURTH ORDER ACCURACY)
200'
210' INSTRUCTIONS--THE INTEGRATION STEP IS H, AND THE
220' SOLUTION IS TABULATED OVER THE INTERVAL T0>=T>=B,
230' IN STEPS OF SIZE L.
240'
250' THE FOLLOWING PROGRAM INPUTS ARE REQUIRED:
260'
270'     510  PRINT "DESIRED OUTPUT TITLE"
280'     530  DEF FNF(X,Y,Z)=[*****]
290'     610  DATA T0, Y0, B
300'     620  DATA n, L
310'     640  LET M=M.0 OR 1.0
320'     690  DEF FNG(T)=[*****]
330'
340' THE OUTPUT WILL BE THE TABULATION OF T, X, AND Y FROM
350' T0 TO B, IF M=0.2. IF M=1.0 IS SELECTED, THE VALUES
360' OF X' AND Y' WILL ALSO BE TABULATED.
370'
380' FOR MODIFICATIONS OF THE PRINT ROUTINE, FOR EXAMPLE TO PLOT
390' THE SOLUTION RATHER THAN TO TABULATE ITS VALUES, THE FOLLOWING
400' LINES, AT LEAST, SHOULD BE MODIFIED:
410'
420'     850  PRINT "VALUE OF T","VALUE OF X","VALUE OF Y"
430'     860  PRINT
440'     900  PRINT T, X, Y
450'     1460 PRINT T, X3, Y7
460'
470'
480' * * * * * MAIN PROGRAM * * * * *
490'
500'     REM INSERT THE PRINTOUT TITLE.
510' PRINT "CCD OUTPUT DIODE RESPONSE TO A STEP FUNCTION INPUT"
511' PRINT
520'     REM DEFINE THE DIFFERENTIAL EQUATION.
530' DEF FNF(X,Y,Z)
540'     LET C=1.4755E-14/SQR(ABS(X-Y))
550'     LET D=2.951E-15/SQR(ABS(Y+25.0))
560'     LET F=C*Z-(2.0E-10)*Y
570'     LET G=C+D+1.618E-13
580'     FNF = F/G

```



```

590 FNEND
600 REM INSERT ITERATION AND TABULATION DATA.
610 DATA 1.4985E-5, -24.3, 4.7015E-5
620 DATA 5.0E-9, 1.0E-6
630 REM SPECIFY THE TYPE OF OUTPUT.
640 LET M=0.0
650 READ T0, Y, B, H, L
660 LET E=1.0/L
670 LET T=T0
680 REM DEFINE THE DRIVING FUNCTION
690 DEF FNG(T)
700 FNG=-25.0
710 IF T<15.0E-6 THEN 740
720 IF T>47.0E-6 THEN 740
730 FNG=-12.0
740 FNEND
750 IF (B-T0)*H>0.0 THEN 770
760 LET H=-H
770 IF (B-T0)*L>0.0 THEN 790
780 LET L=-L
790 LET X=FNG(T)
800 LET Z=(FNG(T+H/2)-FNG(T-H/2))/H
810 REM PRINT INITIAL CONDITIONS.
820 IF M=0.0 THEN 850
830 PRINT " T ", " X ", " Y ", " X' ", " Y' "
840 GO TO 860
850 PRINT "VALUE OF T","VALUE OF X","VALUE OF Y"
860 PRINT
870 IF M=0.0 THEN 900
880 PRINT T, X, Y, Z, FNF(X,Y,Z)
890 GO TO 910
900 PRINT T, X, Y
910 GO TO 1090
920 REM PERFORM THE BASIC ITERATION.
930 LET Z=(FNG(T+H/2)-FNG(T-H/2))/H
940 LET X=FNG(T)
950 LET K1=FNF(X,Y,Z)
960 LET Z1=(FNG(T+H)-FNG(T))/H
970 LET X1=FNG(T+H/2)
980 LET Y1=Y+H*K1/2
990 LET K2=FNF(X1,Y1,Z1)
1000 LET Y2=Y+H*K2/2
1010 LET K3=FNF(X1,Y2,Z1)
1020 LET Y3=Y+H*K3
1030 LET X2=FNG(T+H)
1040 LET Z2=(FNG(T+3*H/2)-FNG(T+H/2))/H
1050 LET K4=FNF(X2,Y3,Z2)
1060 LET Y=Y+H*(K1+2*K2+2*K3+K4)/6.0
1070 LET T=T+H
1080 REM CHECK TO SEE IF IT'S TIME TO PRINT OUT.
1090 IF (T+H-B)*SGN(L)+1.0E-9>=0.0 THEN 1120
1100 LET R=T+H
1110 GO TO 1130

```



```

1120 LET R=B
1130 LET A=INT(E*R)/E+L*(SGN(H)-1.0)/2
1140 IF (A+L-R)*SGN(L)-1.0E-9>=0.0 THEN 1160
1150 LET A=A+L
1160 IF (T-A)*SGN(L)+1.0E-9>=0.0 THEN 1190
1170 LET Q=A
1180 GOSUB 1270
1190 IF R=B THEN 1220
1200 GO TO 930
1210 REM ARE WE DONE YET?
1220 IF ABS(R-A)<0.5E-9 THEN 1250
1230 LET Q=R
1240 GOSUB 1270
1250 STOP
1260 REM ITERATION AND PRINTOUT SUBROUTINE.
1270 LET H1=Q-T
1280 LET Z3=(FNG(T+H1/2)-FNG(T-H1/2))/H1
1290 LET X3=FNG(T)
1300 LET K5=FNF(X3,Y,Z3)
1310 LET Z4=(FNG(T+H1)-FNG(T))/H1
1320 LET X4=FNG(T+H1/2)
1330 LET Y4=Y+H1*K5/2
1340 LET K6=FNF(X4,Y4,Z4)
1350 LET Y5=Y+H1*K6/2
1360 LET K7=FNF(X4,Y5,Z4)
1370 LET Y6=Y+H1*K7
1380 LET X5=FNG(T+H1)
1390 LET Z5=(FNG(T+3*H1/2)-FNG(T+H1/2))/H1
1400 LET K8=FNF(X5,Y6,Z5)
1410 LET Y7=Y+H1*(K5+2*K6+2*K7+K8)/6.0
1420 IF H=0.0 THEN 1460
1430 LET Q=(Y7-Y)/H1
1440 PRINT T, X3, Y7, Z3, Q
1450 GO TO 1470
1460 PRINT T, X3, Y7
1470 RETURN
1480 END

```

READY



## LIST

BIDL01A

23:53

13-DEC-75

```

100 NAME--BIDL01A
110
120 DESCRIPTION--A MODIFICATION OF BIDL01. THIS PROGRAM SOLVES
130 THE INITIAL VALUE PROBLEM DEFINED FOR BIDL01. IN THIS CASE,
140 THE MAXIMUM INPUT VOLTAGE LEVEL IS INCREASED FROM 10 VOLTS
150 TO 20 VOLTS IN STEPS OF 0.25 VOLTS. THE PEAK OUTPUT VOLTAGE
160 IS PRINTED ALONG WITH THE CORRESPONDING INPUT VOLTAGE.
170 THESE VALUES PERMIT A DETERMINATION OF LINEARITY FOR THE
180 SAMPLED OUTPUT REPRESENTED BY THE OUTPUT PULSE.
190
200
210 * * * * * MAIN PROGRAM * * * * *
220
230 REM INSERT THE PRINTOUT TITLE.
240 PRINT "PEAK OUTPUT DIODE VOLTAGE AS A FUNCTION OF"
250 PRINT "      PEAK CHANNEL VOLTAGE"
260 PRINT
270 PRINT "      X PEAK      ","      Y PEAK      "
280 REM DEFINE THE DIFFERENTIAL EQUATION.
290 DEF FNF(X,Y,Z)
300 LET C=1.4755E-14/SQR(ABS(X-Y))
310 LET D=2.951E-15/SQR(ABS(Y+25.0))
320 LET F=C*Z-(2.0E-10)*Y
330 LET G=C+D+1.618E-13
340 FNF = F/G
350 FNEND
360 FOR I=10.0 TO 20.0 STEP 0.25
370 REM INSERT ITERATION AND TABULATION DATA.
380 LET T0=1.4985E-5
390 LET Y=-24.0
400 LET B=4.6985E-5
410 LET H=5.0E-9
420 LET L=4.6985E-5
430 LET E=1.0/L
440 LET T=T0
450 REM DEFINE THE DRIVING FUNCTION
460 DEF FNG(I)
470 FNG=-25.0
480 IF T<15.0E-6 THEN 510
490 IF T>47.0E-6 THEN 510
500 FNG=-1
510 FNEND
520 IF (B-T0)*H>0.0 THEN 540
530 LET H=-H
540 IF (B-T0)*L>0.0 THEN 560
550 LET L=-L

```



```

560 LET X=FNG(T)
570 GO TO 750
580 REM PERFORM THE BASIC ITERATION.
590 LET Z=(FNG(T+H/2)-FNG(T-H/2))/H
600 LET X=FNG(T)
610 LET K1=FNF(X,Y,Z)
620 LET Z1=(FNG(T+H)-FNG(T))/H
630 LET X1=FNG(T+H/2)
640 LET Y1=Y+H*K1/2
650 LET K2=FNF(X1,Y1,Z1)
660 LET Y2=Y+H*K2/2
670 LET K3=FNF(X1,Y2,Z1)
680 LET Y3=Y+H*K3
690 LET X2=FNG(T+H)
700 LET Z2=(FNG(T+3*H/2)-FNG(T+H/2))/H
710 LET K4=FNF(X2,Y3,Z2)
720 LET Y=Y+H*(K1+2*K2+2*K3+K4)/6
730 LET T=T+H
740 REM CHECK TO SEE IF IT'S TIME TO PRINT OUT.
750 IF (T+H-B)*SGN(L)+1.0E-9>=0.0 THEN 780
760 LET R=T+H
770 GO TO 790
780 LET R=B
790 LET A=INT(E*R)/E+L*(SGN(H)-1.0)/2
800 IF (A+L-R)*SGN(L)-1.0E-9>=0.0 THEN 820
810 LET A=A+L
820 IF (T-A)*SGN(L)+1.0E-9>=0.0 THEN 850
830 LET Q=A
840 GOSUB 940
850 IF R=B THEN 880
860 GO TO 590
870 REM ARE WE DONE YET?
880 IF ABS(R-A)<0.5E-9 THEN 910
890 LET Q=R
900 GOSUB 940
910 NEXT I
920 STOP
930 REM ITERATION AND PRINTOUT SUBROUTINE.
940 LET H1=Q-T
950 LET Z3=(FNG(T+H1/2)-FNG(T-H1/2))/H1
960 LET X3=FNG(T)
970 LET K5=FNF(X3,Y,Z3)
980 LET Z4=(FNG(T+H1)-FNG(T))/H1
990 LET X4=FNG(T+H1/2)
1000 LET Y4=Y+H1*K5/2
1010 LET K6=FNF(X4,Y4,Z4)
1020 LET Y5=Y+H1*K6/2

```



```

1030 LET K7=FNF(X4,Y5,Z4)
1040 LET Y6=Y+H1*K7
1050 LET X5=FNG(T+H1)
1060 LET Z5=(FNG(T+3*H1/2)-FNG(T+H1/2))/H1
1070 LET K8=FNF(X5,Y6,Z5)
1080 LET Y7=Y+H1*(K5+2*K6+2*K7+K8)/6.0
1090 PRINT X3, Y7
1100 RETURN
1110 END

```

READY



## LIST

BIDL02

01:02

04-DEC-75

```

100' NAME--BIDL02
110'
120' A PROGRAM TO FIT A CURVE THROUGH A SET OF DATA
130' BY THE METHOD OF LEAST SQUARES.
140'
150' N INDICATES THE TYPE OF CURVE TO BE USED TO FIT THE DATA.
160'
170' THE POWER FUNCTION  $Y=A \cdot X^B$  WILL BE SELECTED IF  $N=0$ .
180'
190' THE EXPONENTIAL FUNCTION  $Y=A \cdot \exp(B \cdot X)$  WILL BE SELECTED IF  $N=1$ .
200'
210' THE POLYNOMIAL  $Y=C(1)+C(2) \cdot X+C(3) \cdot X^2+\dots+C(10) \cdot X^9$  WILL BE
220' SELECTED IF  $N$  EXCEEDS 1. ( $N$  WILL INDICATE THE DEGREE OF THE
230' POLYNOMIAL. FOR EXAMPLE,  $N=3$  INDICATES A SECOND-DEGREE POLY-
240' NOMIAL. NOTE THAT  $N$  IS THE NUMBER OF CONSTANTS IN THE
250' POLYNOMIAL--HENCE,  $N$  CANNOT EXCEED TEN.
260'
270' THE PROGRAM REQUIRES THE FOLLOWING INPUTS:
280'
290' 570 LET  $M=[***]$  THE NUMBER OF DATA PAIRS, NOT TO
300' EXCEED 100 POINTS.
310' 580 LET  $N=[**]$  THE TYPE OF CURVE TO BE FITTED AS
320' DISCUSSED ABOVE.  $N$  CANNOT EXCEED
330' 10 OR  $M$  WHICHEVER IS SMALLER.
340' 590 LET  $IO=[*]$  THE DESIRED OUTPUT FORM, 1 OR 2.
350' 600 DATA  $X(1), Y(1), X(2), Y(2)$  THE DATA TO BE FITTED
360' TO IN PAIRS,  $X$  AND  $Y$ , AS
370' 700 DATA  $X(M), Y(M)$  MANY AS WILL FIT A LINE.
380' 710 PRINT "THE TITLE DESIRED ON THE OUTPUT PRINTOUT"
390'
400' WITHIN THE PROGRAM, THE FOLLOWING DATA IS CONTAINED:
410'
420'  $A(I,J)$ =THE COEFFICIENTS OF THE UNKNOWN CONSTANTS
430'  $C(J)$  =THE UNKNOWN CONSTANTS THAT DEFINE THE FITTED CURVE.
440'  $D(J)$  =THE RIGHT HAND TERMS OF THE SIMULTANEOUS EQUATIONS.
450'
460' IF  $IO$  IS 1.0, THE UNKNOWN CONSTANTS AND THE DATA POINTS ARE
470' PRINTED OUT. IF  $IO$  IS 2.0, THE SYSTEM OF LINEAR EQUATIONS
480' IS PRINTED, AS WELL AS THE UNKNOWN CONSTANTS AND THE DATA
490' POINTS. THE SUM OF THE SQUARES OF THE ERRORS IS ALWAYS
500' PRINTED.
510'
520'

```



```

530 * * * * * MAIN PROGRAM * * * * *
540
550 DIM A(10,10), C(10), D(10), X(100), Y(100)
560 REM READ INPUT DATA.
570 LET M=41
580 LET N=4
590 LET I0=1
600 DATA 10.0, 22.4928, 10.25, 22.5010, 10.5, 22.5091, 10.75, 22.5173
610 DATA 11.0, 22.5256, 11.25, 22.5338, 11.5, 22.5421, 11.75, 22.5504
620 DATA 12.0, 22.5558, 12.25, 22.5642, 12.5, 22.5726, 12.75, 22.5809
630 DATA 13.0, 22.5925, 13.25, 22.6010, 13.5, 22.6096, 13.75, 22.6182
640 DATA 14.0, 22.6268, 14.25, 22.6355, 14.5, 22.6443, 14.75, 22.6530
650 DATA 15.0, 22.6618, 15.25, 22.6707, 15.5, 22.6796, 15.75, 22.6886
660 DATA 16.0, 22.6976, 16.25, 22.7067, 16.5, 22.7158, 16.75, 22.7250
670 DATA 17.0, 22.7343, 17.25, 22.7436, 17.5, 22.7530, 17.75, 22.7625
680 DATA 18.0, 22.7721, 18.25, 22.7818, 18.5, 22.7916, 18.75, 22.8016
690 DATA 19.0, 22.8115, 19.25, 22.8216, 19.5, 22.8319, 19.75, 22.8423
700 DATA 20.0, 22.8529
710 PRINT "OUTPUT VOLTAGE AS A FUNCTION OF INPUT VOLTAGE"
720 PRINT
730 FOR K=1 TO M
740 READ X(K)
750 READ Y(K)
760 NEXT K
770 REM CALCULATE LOGARITHMS OF INPUT ORDINATE DATA IF
780 REM POWER OR EXPONENTIAL CURVE IS BEING FITTED.
790 IF N>=2.0 THEN 970
800 FOR K=1 TO M
810 IF Y(K)>0.0 THEN 850
820 PRINT "NEGATIVE VALUES FOR Y: CANNOT USE A POWER FUNCTION OR"
830 PRINT "AN EXPONENTIAL FIT."
840 STOP
850 LET Y(K)=LOG(Y(K))
860 NEXT K
870 REM CALCULATE LOGARITHMS OF INPUT ABSCISSA DATA
880 REM IF A POWER CURVE IS BEING FITTED.
890 IF N=1.0 THEN 970
900 FOR K=1 TO M
910 IF X(K)>0.0 THEN 940
920 PRINT "NEGATIVE VALUES FOR X: CANNOT USE A POWER FUNCTION FIT."
930 STOP
940 LET X(K)=LOG(X(K))
950 NEXT K
960 REM CALCULATE THE ELEMENTS OF THE A-MATRIX AND THE D-VECTOR.
970 LET N1=N
980 IF N1>=2.0 THEN 1000
990 LET N1=2.0
1000 FOR I=1 TO N1
1010 FOR J=1 TO N1
1020 IF (I+J)>2.0 THEN 1050
1030 LET A(I,J)=0
1040 GO TO 1090
1050 LET A(I,J)=0.0

```



```

1060 FOR K=1 TO M
1070   LET A(I,J)=A(I,J)+X(K)^(I+J-2)
1080 NEXT K
1090 NEXT J
1100   LET D(I)=A*I
1110 FOR K=1 TO M
1120   IF I>1.0 THEN 1150
1130   LET D(I)=D(I)+Y(K)
1140   GO TO 1160
1150   LET D(I)=D(I)+Y(K)*X(K)^(I-1)
1160 NEXT K
1170 NEXT I
1180   REM WRITE THE OPTIONAL OUTPUT IF I=2.
1190   IF I<2.0 THEN 1300
1200   PRINT "COEFFICIENTS IN THE SYSTEM OF LINEAR EQUATIONS:"
1210   PRINT
1220   MAT PRINT A
1230   PRINT
1240   PRINT "THE RIGHT HAND COLUMN VECTOR IS:"
1250   PRINT
1260   FOR I=1 TO N1
1270   PRINT D(I)
1280 NEXT I
1290   REM SOLVE THE SYSTEM OF SIMULTANEOUS LINEAR EQUATIONS.
1300 GO SUB 1890
1310   REM WRITE THE OUTPUT.
1320   PRINT
1330 IF N>=1.0 THEN 1370
1340   LET C0=EXP(C(1))
1350   PRINT "POWER FUNCTION CURVE FIT: Y=";C0;"*x^";C(2)
1360 GO TO 1530
1370 IF N>1.0 THEN 1410
1380   LET C0=EXP(C(1))
1390   PRINT "EXPONENTIAL CURVE FIT: Y=";C0;"*EXP(";C(2);"*x)"
1400 GO TO 1530
1410 IF N=10.0 THEN 1460
1420   LET N2=N+1
1430 FOR I=N2 TO 10
1440   LET C(I)=A*I
1450 NEXT I
1460   PRINT "POLYNOMIAL CURVE FIT:"
1470   PRINT
1480   PRINT "Y=(";C(1);")+(";C(2);")*x+ (";C(3);")*x^2+...";
1490   PRINT "      +(";C(4);")*x^3+(";C(5);")*x^4+...";
1500   PRINT "      +(";C(6);")*x^5+(";C(7);")*x^6+...";
1510   PRINT "      +(";C(8);")*x^7+(";C(9);")*x^8+...";
1520   PRINT "      +(";C(10);")*x^9"
1530   PRINT
1540   REM WRITE OUT THE INPUT VALUES OF X AND Y, AND THE
1550   REM CORRESPONDING CALCULATED VALUES OF Y.
1560   IF N>=2.0 THEN 1640
1570 FOR K=1 TO M
1580   LET Y(K)=EXP(Y(K))
1590 NEXT K

```



```

1600 IF N=1.0 THEN 1640
1610 FOR K=1 TO M
1620 LET X(K)=EXP(X(K))
1630 NEXT K
1640 PRINT "DATA POINTS AND CALCULATED VALUES OF Y"
1650 PRINT
1660 PRINT "VALUE OF X","VALUE OF Y","CALCULATED Y"
1670 PRINT
1680 LET S0=0.0
1690 FOR K=1 TO M
1700 IF N>=1.0 THEN 1730
1710 LET Z4=C0*X(K)+C(2)
1720 GO TO 1810
1730 IF N>1.0 THEN 1760
1740 LET Z4=C0*EXP(C(2)*X(K))
1750 GO TO 1810
1760 LET Z=C(1)+C(2)*X(K)+C(3)*X(K)^2
1770 LET Z1=C(4)*X(K)^3+C(5)*X(K)^4
1780 LET Z2=C(6)*X(K)^5+C(7)*X(K)^6
1790 LET Z3=C(8)*X(K)^7+C(9)*X(K)^8
1800 LET Z4=Z+Z1+Z2+Z3+C(10)*X(K)^9
1810 LET S0=S0+(Z4-Y(K))^2
1820 PRINT X(K), Y(K), Z4
1830 NEXT K
1840 REM WRITE THE ERROR BETWEEN INPUT AND CALCULATED POINTS.
1850 PRINT
1860 PRINT "THE SUM OF THE SQUARE OF THE ERRORS =" ; S0
1870 STOP
1880 REM SUBROUTINE TO SOLVE SIMULTANEOUS LINEAR EQUATIONS.
1890 FOR I=1 TO N1
1900 FOR K=1 TO N1
1910 IF K=1 THEN 2000
1920 LET C0=-A(K,I)/A(1,I)
1930 FOR J=1 TO N1
1940 LET A(K,J)=A(K,J)+C0*A(1,J)
1950 IF J=1.0 THEN 1970
1960 GO TO 1990
1970 LET A(K,J)=0.0
1980 NEXT J
1990 LET D(K)=D(K)+C0*D(1)
2000 NEXT K
2010 LET C0=A(1,1)
2020 FOR J=1 TO N1
2030 LET A(1,J)=A(1,J)/C0
2040 NEXT J
2050 LET A(1,1)=1.0
2060 LET D(1)=D(1)/C0
2070 NEXT I
2080 FOR I=1 TO N1
2090 LET C(1)=D(1)
2100 NEXT I
2110 RETURN
2120 END

```



## LIST

510L43

23:19

84-DEC-75

```

100 NAME--510L43
110
120 DESCRIPTION--A PROGRAM TO EVALUATE THE OUTPUT VOLTAGE
130 OF A MOSFET SOURCE FOLLOWER WITH THE INPUT FROM A
140 CCD CHANNEL THROUGH A REVERSE BIASED DIODE. THE CCD
150 CHANNEL VOLTAGE WILL BE X. THE INPUT TO THE SOURCE
160 FOLLOWER WILL BE V1, THE OUTPUT OF THE SOURCE FOLLOWER
170 IS Y.
180
190 THE MOSFET INPUT VOLTAGE IS APPROXIMATED BY THE
200 POLYNOMIAL RELATIONSHIP:
210
220  $V1 = -(A1 + B1 * X + C1 * X^2 + D1 * X^3)$ 
230
240 THE MOSFET DRAIN-SOURCE CURRENT IS APPROXIMATED BY:
250
260  $I = -K * (V1 - Y - V0)^2$ 
270
280 WHERE:
290     K = THE GAIN PARAMETER IN AMPERE/VOLT2
300     V0 = THE THRESHOLD VOLTAGE IN VOLTS
310
320 THE SOURCE FOLLOWER LOAD RESISTANCE IS R.
330
340
350 * * * * * MAIN PROGRAM * * * * *
360
370 PRINT "OUTPUT OF SOURCE FOLLOWER AS A FUNCTION OF"
380 PRINT "    CHANNEL VOLTAGE IN CCD"
390 PRINT
400 PRINT "CHANNEL","OUTPUT ","    IN"
410 PRINT "VOLTAGE","VOLTAGE","SATURATION"
420 PRINT
430 LET K=2.2032E-6
440 LET V0=-1.76466
450 LET R=5.0E 4
460 LET A1=22.150
470 LET B1=3.8094E-2
480 LET C1=-5.15105E-4
490 LET D1=2.33133E-5
500 LET E=-25.0
510 FOR X=10 TO 20 STEP 0.25
520 LET C2=D1*X+C1
530 LET B2=C2*X+B1
540 LET V1=B2*X+A1
550 LET V1=-V1

```



```

560 LET B=2*(V0-V1)+1.0/(1+R)
570 LET C=V1^2+V0^2-2*V1*V0
580 LET X1=-X
590 LET Y=SQR(B^2-4*C)
600 LET Y=(-B+Y)/2.0
610 LET L=ABS(V1-Y-V0)
620 LET J=ABS(E-Y)
630 IF L<=J THEN 660
640 PRINT X1, Y, "NO"
650 GO TO 670
660 PRINT X1, Y, "YES"
670 NEXT X
680 STOP
690 END

```

READY



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Thesis

B5115

c.1

Biddle

Charge-coupled de-  
vices for analog sig-  
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a circuit study.

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Charge-coupled devices for analog signal



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